Ultra Efficient Dual Sources Energy Manager with MPPT/Constant Voltage, Regulated Buck Output and 5 V CC/CV Charger

Features and Benefits

Dual sources inputs
- Optimized boost operation for each source.
- Efficiency above 90 % on each source.
- Harvests from 110 mV / 2 µW after cold start.
- Simultaneous harvesting from both sources.
- Up to 135 mA current extracted from the harvester.

MPPT and constant voltage modes
- Both modes are available for both sources to ensure optimal harvesting from a multiple combinations of harvesters (PV cells, RF, vibration, pulsed sources...).

Cold start from 275 mV / 1.5 µW input
- Startup at ultra-low power from either harvesting source input.

Selectable overdischarge and overcharge protection
- Supports various types of rechargeable batteries (LiC, Li-ion, LiPo, Li-ceramic pouch...).

Regulated output for application circuit
- Buck regulator with efficiency above 90 %.
- Selectable output voltage between 0.6 V and 2.5 V.
- Output current up to 100 mA.

Thermal monitoring
- Battery protection against over-temperature and under-temperature during charging and discharging, independently.

Power meter
- Measures how much energy has been transferred to the battery by each source and the energy drained from the battery to supply the application circuit.

System configuration by GPIO or I²C communication
- All settings are dynamically configurable through GPIO or I²C (Fast Mode Plus).
- System data is available through I²C.

Shipping mode
- Disables charging and discharging battery during shipment.

External 5 V charging capability
- Extra charging input for 5 V power supplies.
- CC/CV charging with configurable current limit in CC mode (max. 135 mA).
- Provides a fast charging alternative when no source is available for a long time.

Applications

Remote Controls	eReader
PC Peripherals	Electronic Shelf Labels
Asset Tracking	Indoor Sensors

Description

The AEM13920 is a fully integrated and compact power management circuit that extracts DC power from two harvesting sources to store energy in a rechargeable battery and supply an application circuit. A 5 V input can also be used to charge the battery (e.g. if the battery gets depleted). This compact and ultra-efficient battery charger allows for extending battery lifetime and eliminating the primary energy storage in a large range of applications.

Both sources implement Maximum Power Point Tracking (MPPT) as well as constant source voltage regulation features, allowing for harvesting the maximum power available from each source to charge the storage element.

With its unique cold-start circuit, it can start operating with an input voltage as low as 275 mV (min. 1.5 µW power).

The configurable protection levels determine the storage element voltage protection thresholds to avoid overcharging and overdischarging the storage element and thus damaging it. No external components are required to set those levels.

Thermal monitoring protects the storage element. Average Power Monitoring system (APM) allows the application circuit to get a measure of the energy harvested from each source to the battery and from the battery to the application circuit. A shipping mode is available to avoid charging and discharging of the storage element during shipping or storage.

A buck regulator with selectable output voltage allows an application circuit to be supplied with high efficiency.

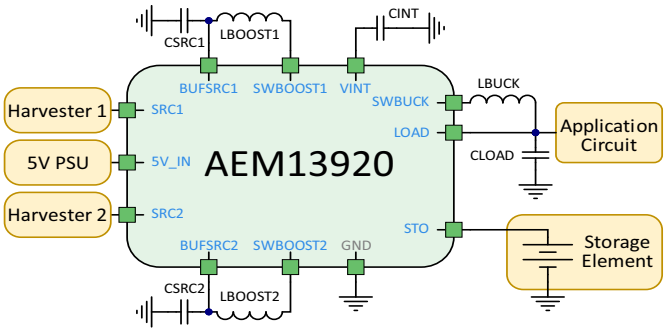
I²C communication allows users to control every setting of the AEM13920 from the application circuit MCU.

Device Information

Part Number	Package	Body size
10AEM13920J0000	QFN 40-pin	5x5mm

Evaluation Board

Part number
2AAEM13920Jxxxx



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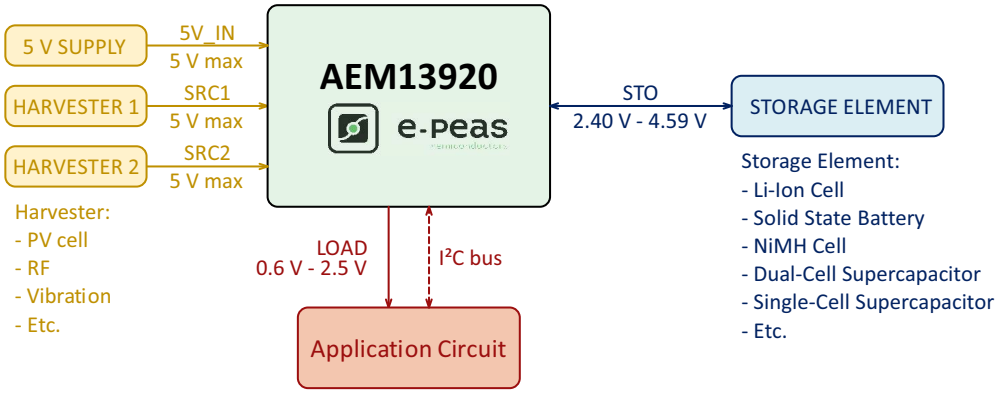


Figure 1: Simplified schematic view

1. Introduction

The AEM13920 is a full-featured energy efficient power management circuit able to harvest energy from two energy sources (connected to SRC1 and/or SRC2) to supply an application circuit (connected to LOAD) and use any excess of energy to charge a storage element (connected to STO). The storage element can also be charged from a 5 V power supply. This is done with a minimal bill of material.

The heart of the AEM13920 is two switching boost converters for energy harvesting and a buck converter for supplying the load. Both have high power conversion efficiency.

The AEM13920 can be configured either by configuration pins or by a set of registers accessed through an I²C bus. Furthermore, some advanced configurations are accessible only through the I²C registers.

A 5 V power input 5V_IN allows for charging the storage element. This is done using a CC/CV (constant current / constant voltage) method. The CC phase maximum current can be configured between 13.5 mA and 135 mA with an external resistor.

At first start-up, as soon as a required cold-start voltage of 275 mV and a sparse amount of power of at least 1.5 µW is available at SRCx (SRC1 or SRC2), the AEM13920 coldstarts. After the cold start, the AEM13920 extracts the power available from the source if the working input voltage is at least 100 mV higher than $V_{SRCx,REG}$. Cold start can also be done from the 5 V power supply input 5V_IN.

The storage element protection levels are configured through

The storage element protection levels are configured through three configuration pins (STO_CFG[2:0]), from which the user can select a specific operating mode out of 8 modes that cover most application requirements without any dedicated external component. If none of those 8 modes fit the user's storage element, the voltage thresholds can also be configured individually through I²C registers to allow the user to define a mode with custom specifications.

The ST_STO status pin provides information about the voltage level of the storage element, and thus about its readiness to supply an application.

Both SRCx inputs of the AEM13920 can work in Maximum Power Point tracking mode (MPPT) or as constant voltage mode. Those modes are configured with a dedicated pin SRCx_MODE or through the I²C registers.

When in MPPT mode, the Maximum Power Point (MPP) ratio is configurable thanks to three configuration pins (SRCx_CFG[2:0]) and ensures an optimum biasing of the harvester to maximize power extraction. Depending on the harvester, it is possible to adapt the timings of the MPP evaluations with the two configuration pins (SRCx_CFG[4:3]) that sets the periodicity and the duration of the MPP evaluation. The MPP ratio and the MPP timings can also be configured through the I²C registers.

When in constant voltage mode, the source regulation voltage $V_{SRCx,REG}$ can be configured thanks to four configuration pins (SRCx_CFG[4:0]). The constant voltage can also be configured with higher precision through the I²C registers.

If the storage element is sufficiently charged, the buck converter provides a regulated voltage output on the LOAD pin, allowing for supplying an application circuit. The regulated voltage can be set through the LOAD_CFG[2:0] pins or through the I²C registers.

A shipping mode can be enabled through the SHIP_MODE pin, disabling the boost converters, the buck converter as well as the 5 V input, thus preventing any charge or discharge of the battery.

2. Pin Configuration and Functions

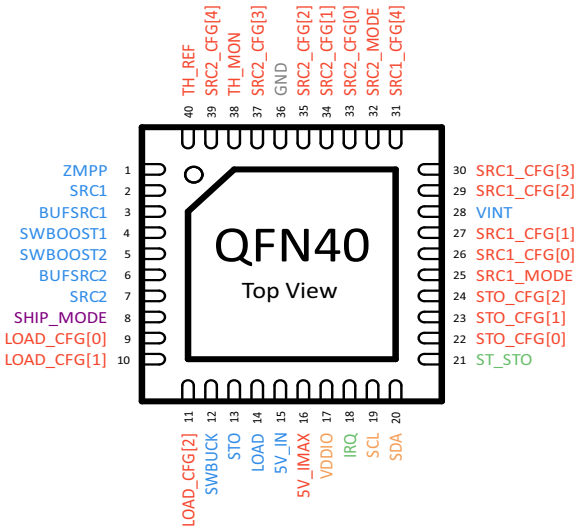


Figure 2: Pinout diagram

NAME	PIN NUMBER	FUNCTION
Power Pins		
SRC1	2	Connection to the energy source harvested by the boost converter #1 and #2 respectively. Connect to GND if not used (typically for single source use of AEM13920).
SRC2	7	
BUFSRC1	3	Connection to an external capacitor buffering the boost converter #1 and #2 inputs respectively. Connect to GND if not used (typically for single source use of AEM13920).
BUFSRC2	6	
SWBOOST1	4	Switching node of the boost converter #1 and #2 respectively. Leave floating if not used (typically for single source use of AEM13920).
SWBOOST2	5	
ZMPP	1	Connection for R_{ZMPP}. Leave floating if not used.
STO	13	Connection to the energy storage element (rechargeable battery).
SWBUCK	12	Switching node of the buck converter. If not used: - Disable buck converter through LOAD_CFG[2:0] pins or BUCKCFG.VOUT register field. - Leave the SWBUCK pin floating.
LOAD	14	Output voltage of the buck converter to supply an application circuit. If not used: - Disable buck converter through LOAD_CFG[2:0] pins or BUCKCFG.VOUT register field. - Leave the LOAD pin floating.
5V_IN	15	Input of the 5 V DC power supply. Leave floating if not used.
VDDIO	17	Supply and voltage reference for the I²C interface, as well as for the IRQ and ST_STO pins. - If used, connect to a DC power supply. - If not used, connect to GND.
VINT	28	Connection for C_{INT} buffering capacitor. AEM13920 internal power supply (do not connect any external circuit on VINT).

Table 1: Pins description (part 1)

NAME		PIN NUMBER	LOGIC LEVEL		FUNCTION
			LOW	HIGH	
Control Pin					
SHIP_MODE		8	GND	STO	Logic input. When HIGH: - Minimum consumption from the storage element. - Storage element charge is disabled (Boost converters are disabled). - Buck (LOAD) is disabled. - Only VINT is charged if energy is available on SRC1 or SRC2. Read as LOW if left floating.
Configuration Pins					
SRC1_MODE		25	GND	VINT	Sets SRCx voltage regulation strategy: - LOW: constant voltage mode. - HIGH: MPPT mode (ratio or ZMPP). Read as HIGH if left floating.
SRC2_MODE		32	GND	VINT	
SRC1_CFG[4:0]	SRC1_CFG[4]	31	GND	VINT	Used for the configuration of SRCx regulation voltage. SRCx_MODE = LOW (constant voltage mode): - SRCx_CFG[4:0] are used to set SRCx constant regulation voltage. SRCx_MODE = HIGH (MPPT ratio mode): - SRCx_CFG[2:0] are used to set SRCx MPPT ratio. - SRCx_CFG[4:3] are used to set SRCx MPPT timings. SRCx_CFG[4:0] are all read as HIGH when left floating.
	SRC1_CFG[3]	30	GND	VINT	
	SRC1_CFG[2]	29	GND	VINT	
	SRC1_CFG[1]	27	GND	VINT	
	SRC1_CFG[0]	26	GND	VINT	
SRC2_CFG[4:0]	SRC2_CFG[4]	39	GND	VINT	
	SRC2_CFG[3]	37	GND	VINT	
	SRC2_CFG[2]	35	GND	VINT	
	SRC2_CFG[1]	34	GND	VINT	
	SRC2_CFG[0]	33	GND	VINT	
STO_CFG[2]		24	GND	VINT	Used to configure the storage element voltage thresholds. Read as HIGH if left floating.
STO_CFG[1]		23	GND	VINT	
STO_CFG[0]		22	GND	VINT	
LOAD_CFG[2]		11	GND	VINT	Used to configure the LOAD output regulation voltage. Read as HIGH if left floating.
LOAD_CFG[1]		10	GND	VINT	
LOAD_CFG[0]		9	GND	VINT	
5V_IMAX		16	Analog Pin		Connection to an external resistor to set the charging current from the 5V_IN supply to STO. Leave floating if the 5V_IN power supply is not used.

Table 2: Pins description (part 2)

NAME	PIN NUMBER	LOGIC LEVEL		FUNCTION
		LOW	HIGH	
TH_REF	40	Analog Pin		Reference voltage for thermal monitoring. Leave floating if not used.
TH_MON	38	Analog Pin		Connection for thermistor voltage divider mid-point. Connect to VINT if not used.
I²C Pins				
SCL	19	GND	VDDIO	Unidirectional serial clock for I²C communication. Connect to GND if not used.
SDA	20	GND	VDDIO	Bidirectional data line for I²C communication. Connect to GND if not used.
IRQ	18	GND	VDDIO	Logic output signal to indicate AEM13920 events to external circuit GPIO. Leave floating if not used.
Status Pin				
ST_STO	21	GND	VDDIO	Logic output. - HIGH when in SUPPLY STATE or in SLEEP STATE. - LOW otherwise. Leave floating if not used.
Other pins				
GND	Exposed Pad, 36			Ground connection, each terminal should be strongly tied to the PCB ground plane.

Table 2: Pins description (part 2)

3. Absolute Maximum Ratings

Parameter	Value
Operating junction temperature	TBD
ESD HBM voltage	TBD
ESD CDM voltage	TBD

Table 3: Absolute maximum ratings

4. Thermal Resistance

Package	θJA	θJC	Unit
TBD	TBD	TBD	°C/W

Table 4: Thermal data

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

5. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power conversion						
$P_{SRCx,CS}$	Minimum source power required for cold start.			1.5[1]		µW
$V_{SRCx,CS}$	Minimum source voltage required for cold start.			0.275		V
V_{MPP}	Target regulation voltage on SRCx when extracting power.	- SRCx_MODE = HIGH.	0.11		4.50	V
$V_{SRCx,REG}$	Target regulation voltage of the source, depending on SRCx_CFG[4:0] configuration or I²C register.	- SRCx_MODE = LOW. - Configured by SRCx_CFG[4:0] pins.	0.14		2.10	V
		- SRCx_MODE = LOW. - Configured by I²C register.	0.11[2]		4.50	V
V_{OC}	Open-circuit voltage of the source.		0.00[3]		5.00	V
V_{5V_IN}	Voltage on the 5V_IN pin to allow for charging the battery.		3.50		5.50	V
$P_{5V\_IN,MIN}$	Minimum power on 5V_IN to start charging the battery.	V_{5V_IN} = 3.50 V		51		µW
		V_{5V_IN} = 5.50 V		80		
$I_{5V,CC}$	Maximum charging current of 5 V charger when in constant current (CC) mode. This is programmed by the resistor on the 5V_IMAX pin.		13.50		135	mA
V_{VDDIO}	Voltage on VDDIO.		1.50		5.00	V
Timing						
$T_{MPPT,SAMPLING}$	Open-circuit duration for the MPP evaluations (see Table 10).	Configured by SRCx_CFG[4:0].	2		256	ms
		Configured by I²C.			512	
$T_{MPPT,PERIOD}$	Time between two MPP evaluations (see Table 10).	Configured by SRCx_CFG[4:0].	0.134		16.38	s
		Configured by I²C.			4.00	
T_{CRIT}	In SUPPLY STATE, the AEM13920 waits for T_{CRIT} before switching to OVDIS STATE when V_{STO} drops below V_{OVDIS}.			2.50		s
$T_{GPIO,MON}$	GPIO reading rate.			2.05		s
$T_{TEMP,MON}$	Temperature monitoring rate.			8.19		s

Table 5: Electrical characteristics (part 1)

1. For V_{SRCx} = 0.275 V. Cold-start duration is typically 3 minutes.
2. The minimum source regulation voltage $V_{SRCx,REG}$ is the default sleep threshold.
3. When the open-circuit voltage is below the source regulation voltage (MPPT or constant voltage), the AEM13920 does not extract power from the source. Voltages down to GND voltage does not damage the AEM13920 though.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Storage element						
V_{STO}	Voltage on the storage element.		2.40[1]		4.59[2]	V
V_{OVDIS}	Minimum voltage accepted on the storage element before stopping to supply LOAD (see Section 9.4).	Configured by STO_CFG[2:0].	2.50		3.50	V
		Configured by I²C.	2.40	18 mV steps	3.58	V
V_{CHRDY}	Minimum voltage accepted on the storage element before starting to supply LOAD in START STATE (see Section 9.4).	Configured by STO_CFG[2:0].	2.55		3.55	V
		Configured by I²C.	2.46	18 mV steps	3.64	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging (see Section 9.4).	Configured by STO_CFG[2:0].	3.50		4.12	V
		Configured by I²C.	2.70	18 mV steps	4.59	V
Internal supply & quiescent current						
V_{INT}	Internal voltage supply.		2.20	2.25	2.30	V
$V_{INT,RESET}$	Minimum voltage on VINT before switching to RESET STATE (from any other state).			2.0		V
$V_{INT,CS}$	Minimum voltage on VINT to allow the AEM13920 to switch from RESET STATE to SENSE STO STATE.			2.3		V
$I_{QSUPPLY}$	Quiescent current on STO in SUPPLY STATE.[3]	Buck enabled (LOAD).		495		nA
		Buck disabled (LOAD).		325		nA
I_{QSLEEP}	Quiescent current on STO in SLEEP STATE.[3]	Buck enabled (LOAD).		375		nA
		Buck disabled (LOAD).		230		nA
$I_{QSHIP,SRCx}$	Quiescent current on STO when the shipping mode functionality is enabled (SHIP_MODE set HIGH).	Energy on SRCx.		10		nA
I_{QSHIP}	Quiescent current on STO when the AEM13920 is off.	No energy on SRCx.		10		nA

Table 6: Electrical characteristics (part 2)

1. As set by the battery overdischarge threshold configuration.
2. As set by the battery overcharge threshold configuration.
3. When neither the boost converters nor the buck converter are running.

6. Recommended Operation Conditions

Symbol	Parameter		Min[1]	Typ	Max[1]	Unit
External components						
L_{BOOSTx}	Inductor of the boost converters.		3.3	33		µH
C_{SRCx}	Capacitor decoupling the BUFSRCx pin.			10	10	µF
L_{BUCK}	Inductor of the buck converter.		3.75	15		µH
C_{LOAD}	Capacitor of the buck converter.		10	22		µF
C_{INT}	Capacitor decoupling the VINT terminal.		5	10		µF
R_{5V_IMAX}	Resistor for configuring the 5V charger current when in constant current mode (CC).		0.37		3.7	kΩ
R_{SDA} R_{SCL}	Pull-up resistors for the I²C interface.			1		kΩ
R_{TH}	NTC thermistor used for thermal monitoring operation.	R0	0	10[2]	250	kΩ
		Beta		3380[2]		K
R_{DIV}	Resistor used to create a resistive divider with R_{TH} for thermal monitoring operation.		4	22[2]	40	kΩ
R_{ZMPP}	Optional - Resistor used for the configuration of the ZMPP function.		33		1M	Ω

Table 7: Recommended external components

1. All minimum and maximum values are real components values, taking into account tolerances, derating, temperatures, voltages and any operating conditions (special care must be taken with capacitor derating).
2. Those values allow for having a default setting at startup of -25 °C for the "cold" threshold and +70 °C for the "hot" threshold, for both charging and discharging.

Symbol	Parameter		
Logic input pins			
SRCx_MODE	Boost source voltage regulation mode.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
SRCx_CFG[4:0]	Boost source voltage regulation settings.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
STO_CFG[2:0]	Storage element voltage thresholds configuration.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
LOAD_CFG[2:0]	Configuration of the LOAD buck output voltage regulation.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to VINT.
SHIP_MODE	Shipping mode enable pin.	Logic LOW	Connect to GND.
		Logic HIGH	Connect to STO.
I²C interface pins			
SCL	I²C clock signal pin.		Pull-up to VDDIO with resistors R_{SCL} and R_{SDA}.
SDA	I²C data signal pin.		

Table 8: Logic input pins and I²C interface pins connections

7. Functional Block Diagram

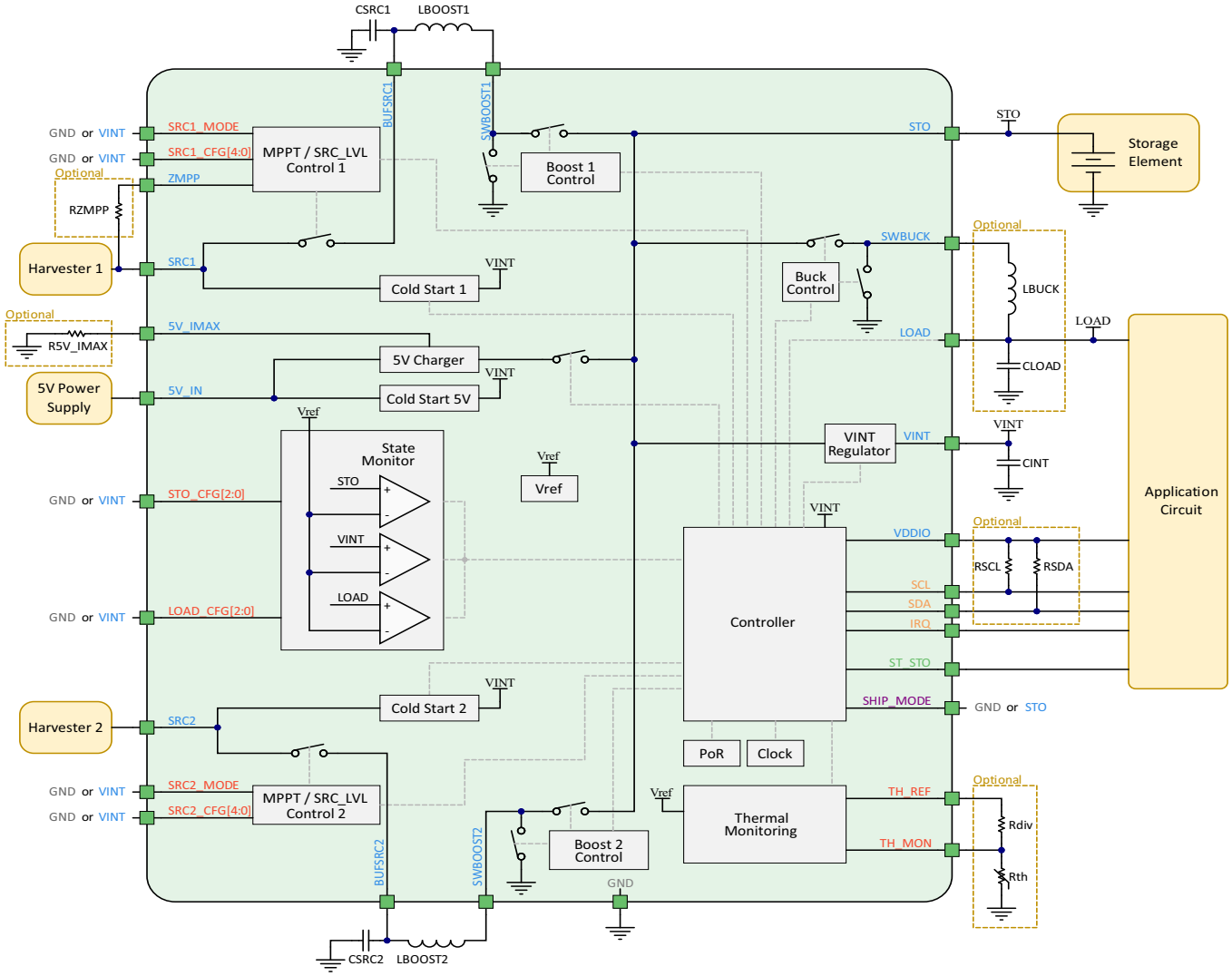


Figure 3: Functional block diagram

8. Theory of Operation

8.1. Cold-Start Circuits

The AEM13920 is able to coldstart from either SRCx or from 5V_IN (see Table 5 for cold-start conditions). The cold-start circuit supplies the AEM13920 internal circuit (connected to VINT) when the device is in RESET STATE, SENSE STO STATE or OVDIS STATE.

See Table 5 for the typical AEM13920 minimum cold-start voltage $V_{SRCx,CS}$ and minimum cold-start power $P_{SRCx,CS}$. Those results have been measured starting with all AEM13920 node discharged expected V_{STO} that is charged above V_{CHRDY}. The cold start is considered to be finished when LOAD is supplied (buck is enabled), meaning that the AEM13920 has switched to SUPPLY STATE.

The time necessary for the AEM13920 to perform a cold start depends on multiple parameters such as:

- V_{SRCx}: the higher the source voltage, the faster the cold start.
- C_{INT} value: the higher the capacitance on VINT, the slower the cold start.

Typical cold-start time may vary between a few minutes for very low V_{SRCx} to a few tens of milliseconds for high V_{SRCx}.

8.2. Boost Converters

Please note that the following explanations apply to both boost converters #1 and #2.

8.2.1. Operation Principle

The boost (step-up) converter raises the voltage available at BUFSRCx to a level suitable for charging the storage element, in the range of 2.40 V to 4.59 V, according to the system configuration. The switching transistors of the boost converter are M2x and M3x. The reactive power component of this converter is the external inductor L_{BOOSTx}.

M1x allows for disconnecting the SRCx pin from BUFSRCx, which happens in the following cases:

- When measuring the source open-circuit voltage, if source mode is MPPT (see Section 8.2.2).
- When the boost converter is disabled through I²C (see Section 9.11.4).
- When AEM13920 is in SLEEP STATE, SENSE STO STATE or RESET STATE (see Section 8.9).
- When temperature is out of range (see Section 8.4).
- When a suitable power supply is connected to the 5V_IN pin (both boosts are disabled in that case).

When the boost converter is extracting energy from the source, M1x is closed, connecting SRCx to BUFSRCx.

Target source regulation voltage can be determined by:

- The MPPT module when SRCx_MODE is HIGH (ratio of open-circuit voltage or target impedance connected to ZMPP (see Section 8.2.2).
- The constant voltage regulation setting when SRCx_MODE is LOW (see Section 8.2.3).

BUFSRCx is decoupled by the capacitor C_{SRC1}, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the STO pin, which voltage is V_{STO}. This node is linked to the output of the boost converter through transistor M3x. When energy harvesting is occurring, the boost converter charges the battery.

The maximum current supplied to the STO pin depends on both the value of L_{BOOSTx} and on the settings of the I²C register field BSTxCFG[4:2], that sets the boost converters timings for charging and discharging L_{BOOSTx}, and thus its peak current $I_{LBOOST,PEAK}$. See Section 9.11.4 for further information, as well as typical combinations of L_{BOOSTx} inductor value and boost converters timings.

While using an energy source is mandatory, using both boost converters is not: user might use a single boost converter or even use the AEM13920 only with the 5 V charger as energy source. The following connections must be done if a boost converter is not used:

- SRCx and BUFSRCx to GND.
- Leave SWBOOSTx floating.

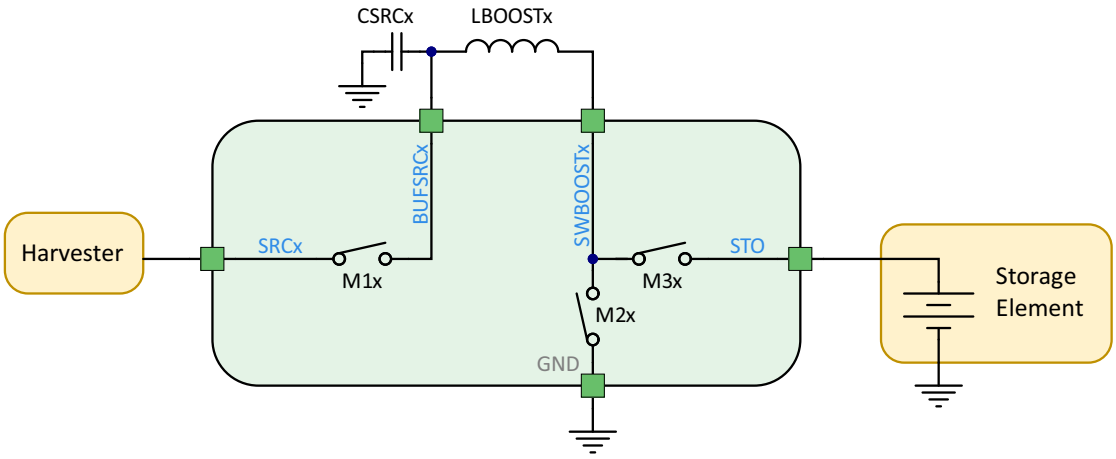


Figure 4: Simplified schematic view of the boost converters

8.2.2. Maximum Power Point Tracking

This section describes the AEM13920 behavior when source regulation mode is MPPT. Switching to this mode is done by setting the SRCx_MODE pin HIGH or by setting SRCxREGU0.MODE I²C register field bit HIGH (see Sections 9.2 and 9.11.2).

The MPPT module is active during START STATE, OVDIS STATE and SUPPLY STATE.

8.2.2.1. Open-Circuit Voltage Ratio

In open-circuit voltage ratio mode, the AEM13920 MPPT relies on the fact that, for several models of harvesters (typ. solar cells), the ratio between the maximum power point voltage (V_{MPP}) and the open-circuit voltage (V_{OC}) is constant for a wide range of harvesting conditions. For a solar cell, that means that V_{MPP} / V_{OC} is constant for any lighting conditions, even though both voltages increase when luminosity increases. Please note that this is valid for a large variety of harvesters, not only solar cells.

The Maximum Power Point (MPP) ratio V_{MPP} / V_{OC} differs from one harvester model to another. User must set the MPP ratio to match the specifications of the harvester model used and thus maximize power extraction. This ratio is set with the configuration pins SRCx_CFG[2:0] (see Section 9.2) or with the I²C interface register field SRCxREGU0.CFG0 (see Section 9.11.2).

The MPPT module evaluates the open-circuit voltage V_{OC} periodically to ensure optimal power extraction at any time. The sampling period $T_{MPPT,PERIOD}$ and sampling duration $T_{MPPT,SAMPLING}$ of the evaluation of V_{OC} are set with the configuration pins SRCx_CFG[4:3] (see Section 9.2) or by configuring fields from the SRCxREGU1 register (see Section 9.11.2).

Every $T_{MPPT,PERIOD}$, the MPPT stops extracting power from the source, waits during $T_{MPPT,SAMPLING}$ for the source to rise to its open-circuit voltage V_{OC}, and measures V_{OC}. The AEM13920 allows for a wide range of V_{MPP} levels, and offers a choice of eight values for the V_{MPP} / V_{OC} ratio.

8.2.2.2. ZMPP

Some harvesters provide better performance when connected to a circuit with constant input resistance. The AEM13920 boost converter #1 MPPT can be set as constant input resistance by enabling the ZMPP function. This can be done by setting all SRC1_CFG[2:0] pins HIGH (see Section 9.2) or by setting the field SRC1REGU0.CFG0 to 0x07 (see Section 9.11.2).

In ZMPP mode, the AEM13920 regulates the input resistance of SRC1 to match the resistance R_{ZMPP} connected to the ZMPP pin. Operation is similar to that of the V_{MPP} / V_{OC} mechanism described in Section 8.2.2.1:

- Every $T_{MPPT,PERIOD}$, the AEM13920 disconnects SRC1 from BUFSRC1, and connects the ZMPP pin to GND, with R_{ZMPP} thus becoming the source load resistance.
- After a $T_{MPPT,SAMPLING}$ delay, the AEM13920 measures the voltage on SRC1, loaded by R_{ZMPP}. The measured voltage is the new SRC1 input regulation voltage.

When in ZMPP mode, $T_{MPPT,SAMPLING}$ is determined as for the V_{MPP} / V_{OC} mode: either by SRC1_CFG[4:3] (see Section 9.2) or by the SRC1REGU1.CFG1 I²C register field (see Section 9.11.2).

Please note that the ZMPP feature in only available on boost converter 1, or when a harvester is connected on both boost converters simultaneously, as described in Section 8.2.5.

In the later case, user must configure the AEM13920 as follows:

- SRC1 and SRC2 as MPPT (SRC1_MODE and SRC2_MODE HIGH).
- SRC1 MPP ratio to ZMPP.
- SRC2 MPP ratio to 100%.
- A single R_{ZMPP} resistor connected between ZMPP and SRC1/SRC2.

Figure 5 illustrates this configuration:

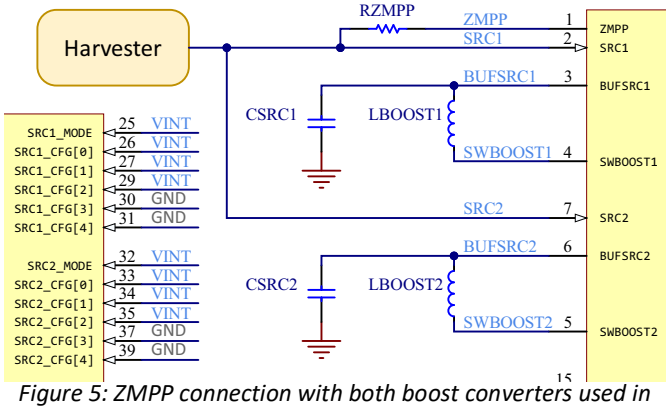


Figure 5: ZMPP connection with both boost converters used in parallel

8.2.3. Source Voltage Regulation

This section describes the AEM13920 behavior when source regulation mode is constant voltage. Switching to this mode is done by setting the SRCx_MODE LOW or by setting SRCxREGU0.MODE I²C register field bit LOW (see Sections 9.3 and 9.11.2).

During START STATE, OVDIS STATE and SUPPLY STATE, the voltage on SRCx is regulated to a voltage configured by the user. The AEM13920 offers a wide choice of values for the source regulation voltage $V_{SRCx,REG}$ (see Section 9.3).

In constant voltage regulation mode, the AEM13920 behaves as follows:

- If the open-circuit voltage V_{OC} of the harvester is lower than $V_{SRCx,REG}$, the AEM13920 does not extract power from the source.
- If SRCx voltage is higher than V_{OC}, the AEM13920 regulates V_{SRCx} to $V_{SRCx,REG}$ and thus extracts power from the source.

8.2.4. Automatic High-Power Mode

When the AEM13920 detects that the energy available on SRCx is high enough, the boost converter automatically switches to high-power mode.

Preventing the AEM13920 to switch to high-power mode may allow to use an inductor with half peak current rating for L_{BOOSTx} (see Section 9.11.4). On the other hand, allowing the AEM13920 to switch to high-power mode increases the maximum current that the AEM13920 can harvest from SRCx to STO.

Automatic high-power mode is enabled by default and can be disabled by setting the BSTxCFG.ENHP register bit to 0 through the I²C interface.

8.2.5. Using Both Boost Converters in Parallel

It is possible to use the two boost converters in parallel to double the current that can be extracted from a single harvester.

To do so, user must configure the AEM13920 as follows:

- Connect the harvester simultaneously on SRC1 and SRC2.
- Configure both boost converters input with identical regulation settings (MPPT with the same ratio or same constant voltage).
- C_{SRC1}, C_{SRC2}, L_{BOOST1} and L_{BOOST2} must all be populated and both boost timings must be configured accordingly.

Please note that ZMPP can be configured to work in that case, see Section 8.2.2.2 for further information.

8.3. Buck Converter

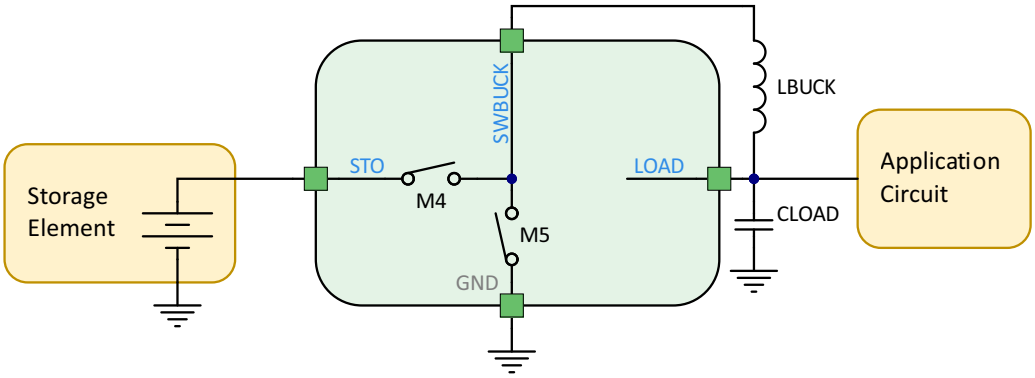


Figure 6: Simplified schematic view of the buck converter

The buck (step-down) converter transfers energy from the battery connected on STO to the regulated LOAD output. The switching transistors of the buck converter are M4 and M5. The reactive power component of this converter is the external inductor L_{BUCK}. LOAD is decoupled by the capacitor C_{LOAD}, which smooths the voltage against the current pulses induced by the consumption of the external circuit connected to LOAD.

Setting the LOAD regulation voltage V_{LOAD} or disabling the buck converter is done through LOAD_CFG[2:0] pins (see Sections 9.5) or I²C register BUCKCFG (see Section 9.11.5).

After cold start and if enabled, the buck converter starts once V_{STO} is higher than V_{CHRDY}. It stays enabled, and thus regulates V_{LOAD}, until V_{STO} drops below V_{OVDIS}.

The maximum current supplied to the LOAD pin depends on both the value of L_{BUCK} and the setting of the I²C register field BUCKCFG[5:3], that sets the buck converter timings for charging and discharging L_{BUCK}, and thus its peak current $I_{LBUCK,PEAK}$. See Section 9.11.5 for further information and typical combinations of L_{BUCK} inductor value and buck converter timings.

Using the buck converter is not mandatory. If not used, user must do the following:

- Connect all LOAD_CFG[2:0] to GND (LOW) to disable the buck converter.
- Leave SWBUCK and LOAD floating.

When the difference between V_{STO} and V_{LOAD} is too small for the buck converter to keep working properly, it switches to "bang-bang" controlled converter mode:

- When V_{LOAD} is too low, a switch connects STO directly to LOAD, making V_{LOAD} rise.
- When V_{LOAD} is too high, the controller disconnects STO and LOAD so that V_{LOAD} decreases.

This happens when the following condition is satisfied:

$$V_{STO} - V_{LOAD} < 0.25V$$

In that case, efficiency is lower than in buck mode (see Figure XXX).

8.4. Thermal Monitoring

Thermal monitoring allows for protecting the storage element. Enabling this functionality requires the use of a resistor (R_{DIV}) and a NTC thermistor (R_{TH}), forming a resistive divider. See Figure 9 for connections of those external components. The TH_REF terminal allows for applying a reference voltage to the resistive divider while TH_MON is the measuring point. The temperature evaluation is done periodically every $T_{TEMP,MON}$ (see Table 5). To spare power, the divider is biased only during this evaluation. See Section 9.6 for further information about thermal monitoring configuration.

Thermal monitoring is optional, if not used connect TH_MON to VINT and leave TH_REF floating.

8.5. Average Power Monitoring

The Average Power Monitoring (APM) module allows for evaluating the energy transfer through a power converter. The AEM13920 implements three different APM modules, evaluating the power transferred on different paths:

- APMSRC1: power transferred to STO from SRC1 (boost #1 power converter).
- APMSRC2: power transferred to STO from SRC2 (boost #2 power converter).
- APMLOAD: power transferred from STO to LOAD (buck power converter).

Please note that all three measures are related to STO (energy provided to the storage element or provided by it).

All three APM modules work the same, so for the following explanations, let us define the following:

- APM_IN as the input node measured by the APM module.
- APM_OUT as the output node measured by the APM module.

The APM module is able to determine the transferred energy by counting the number of current pulses transferred from APM_IN to APM_OUT by the DCDC converter over a configurable time window, and thus evaluate the corresponding energy.

Two modes are available: Pulse Counter mode and Power Meter mode.

The APM module behavior is described in Figure 7:

- **Phase A**:
  - **Pulse Counter mode**: APM module counts the number of DCDC pulses happening during T_A.
  - **Power Meter mode**: APM module integrates the energy transferred from APM_IN to APM_OUT during T_A.
- **Phase B**: APM module waits during $T_B = T_A$.
- IRQ: a rising edge is triggered on the IRQ pin, if IRQEN1.APMDONE field is set to 1 (see Section 9.11.11). A rising edge on IRQ along with the IRQFLAG1.APMDONE field set to 1 indicates to the user that a new value is available and ready to be read in the APM Data Register (see Section 9.11.15).

Please note that all three APM modules are synchronous: T_A and T_B take place at the same time for all modules. Furthermore, if IRQEN1.APMDONE is set, when IRQ rises and IRQFLG1.APMDONE is set, new data for all enabled APM modules is available.

Refer to Section 9.11.15 for further details about how to set modes, how to convert registers value to Joule and how to set T_A.

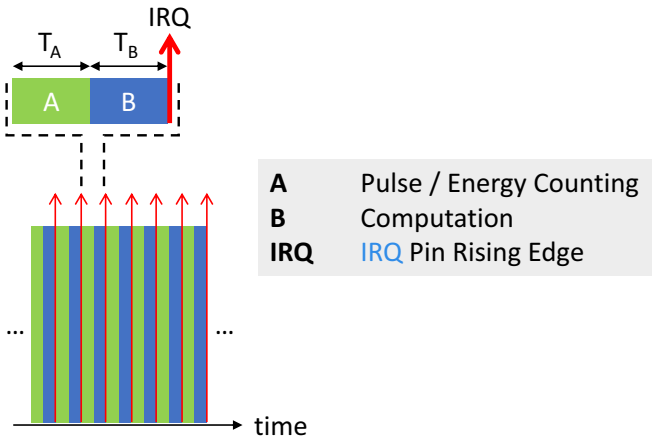


Figure 7: Average Power Monitoring description

8.6. IRQ Pin

The IRQ pin allows users to get an interrupt on the application circuit (rising edge on IRQ pin), triggered by various AEM13920 events. At startup, the only interrupt that is enabled is I2CRDY, signaling that the AEM13920 has finished to coldstart and thus, that it is out from RESET STATE. Other interrupts can be enabled by writing the IRQEN0 and IRQEN1 registers (see Section 9.11.11).

When the IRQ pin shows a rising edge, the interrupt source can be determined by reading the IRQFLG0 and IRQFLG1 registers (see Section 9.11.12). IRQ pin is reset when the corresponding IRQFLGx register is read.

8.7. 5V Charger

The AEM13920 is equipped with a 5 V charger for fast charging of the battery connected on the STO pin. When a voltage higher than 3.5 V is detected on the 5V_IN pin, the charger starts charging the battery, implementing a constant current / constant voltage operation (CC/CV):

- Constant current (CC) operation:
  - When $V_{STO} < V_{OVCH}$ - 50 mV.
  - Battery charging current $I_{5V,CC}$ is configured by the value of the R_{5V_IMAX} resistor connected to the 5V_IMAX pin (see Section 9.7 for further details about R_{5V_IMAX} configuration). $I_{5V,CC}$ range is from 13.5 mA to 135 mA.
- Constant voltage (CV) operation:
  - When V_{OVCH} - 50 mV < V_{STO} < V_{OVCH}.
  - The charging current $I_{5V,CV}$ gradually decreases to zero as the V_{STO} reaches V_{OVCH}.

Using the 5 V charger is not mandatory. When not used, leave both 5V_IN and 5V_IMAX pins floating.

8.8. Shipping Mode

The shipping mode feature allows for forcing the AEM13920 in RESET STATE (see Figure 8 and Section 8.9.1), thus disabling all AEM13920 functionalities including both boost converters, the buck converter and the 5 V charger. Only VINT is charged if energy is available from SRCx. The battery is no longer charged or discharged.

See Section 9.8 for shipping mode enabling and disabling.

8.9. State Machine Description

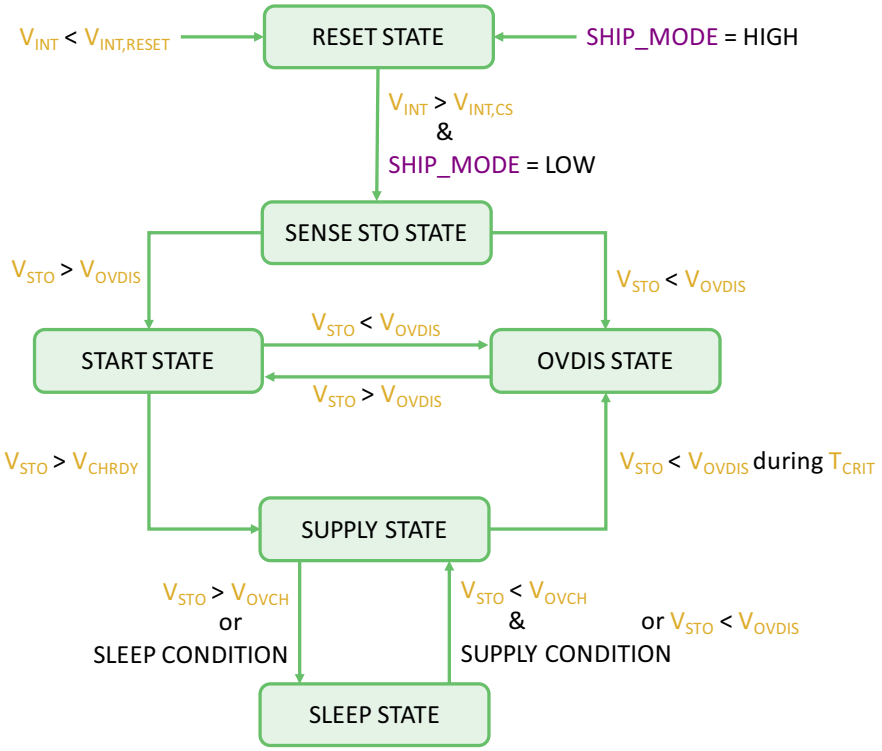


Figure 8: AEM13920 state machine

8.9.1. Reset State

The AEM13920 enters RESET STATE if one of the following is true:

- V_{INT} is below 2 V.
- shipping mode is enabled (SHIP_MODE is HIGH).

In RESET STATE, the AEM13920 behaves as follows:

- The AEM13920 is performing a cold start to make V_{INT} rise to 2.3 V. Cold start can be done from any of the following energy sources:
  - SRCx (V_{SRCx} > 0.275 V and $P_{SRCx,CS}$ > 1.5 µW).
  - 5V_IN (V_{5V_IN} > 3.5 V).
- The AEM13920 internal circuit, connected on VINT, is supplied by SRCx or 5V_IN. No current is drawn from the battery.
- ST_STO is LOW.

The AEM13920 stays in RESET STATE until the power available on either SRCx meets the cold-start requirements long enough to make V_{INT} reach 2.3 V (see Table 5). Then:

- If shipping mode is disabled (SHIP_MODE is LOW), the AEM13920 reads the value on all configuration pins and switches to SENSE STO STATE.
- If shipping mode is enabled (SHIP_MODE is HIGH), the AEM13920 stays in RESET STATE until shipping mode is disabled by setting SHIP_MODE LOW. Please note that SHIP_MODE is read every $T_{GPIO,MON}$ (about 2 s).

Please note that, from any state, the AEM13920 will switch to RESET STATE if V_{INT} drops below 2 V.

8.9.2. Sense STO State

In SENSE STO STATE, a first measure of V_{STO} is performed by the AEM13920.

- If V_{STO} > V_{OVDIS}, the AEM13920 switches to START STATE.
- If V_{STO} < V_{OVDIS}, the AEM13920 switches to OVDIS STATE.
- The AEM13920 internal circuit, connected on VINT, is supplied by SRCx or 5V_IN. If not enough power is available on either of those pins, the AEM13920 switches to RESET STATE. No current is drawn from the battery.
- ST_STO is LOW.

In SENSE STO STATE, none of the DCDC converters are running. This state lasts for about 2 ms.

8.9.3. Start State

When in SENSE STO STATE, the AEM13920 switches to START STATE if V_{STO} is above V_{OVDIS}.

In START STATE, the AEM13920 behaves as follows:

- The battery connected on STO is charged by the boost converters or by the 5V charger, until V_{STO} reaches V_{CHRDY}.
- The AEM13920 internal circuit connected on VINT is supplied by the battery regardless of the power available on SRCx or 5V_IN.
- The buck converter (LOAD) is disabled.
- ST_STO is LOW.

8.9.4. Supply State

When in START STATE, the AEM13920 switches to SUPPLY STATE if V_{STO} is above V_{CHRDY}.

In SUPPLY STATE, the AEM13920 behaves the same as when in START STATE, but with the following differences:

- The buck converter driving LOAD is enabled (if enabled by the user).
- ST_STO is HIGH.

When in SUPPLY STATE, the AEM13920 switches to SLEEP STATE if one of the following conditions is met:

- V_{STO} > V_{OVCH}.
- SLEEP CONDITION (see Section 8.9.6).

8.9.5. OVDIS State

The AEM13920 switches to OVDIS STATE if:

- V_{STO} is below V_{OVDIS} when in SENSE STO STATE or START STATE.
- V_{STO} remains below V_{OVDIS} for more than T_{CRIT} when in SUPPLY STATE.

In OVDIS STATE, the AEM13920 behaves as follows:

- The battery connected on STO is charged by the boost converters and/or by the 5V charger, until V_{STO} exceeds V_{OVDIS}.
- The AEM13920 internal circuit, connected on VINT, is supplied by SRCx or 5V_IN. If not enough power is available on either of those pins, the AEM13920 switches to RESET STATE. No current is drawn from the battery.
- The buck converter (LOAD) is disabled.
- ST_STO is LOW.

8.9.6. Sleep State

SLEEP STATE allows for reducing the AEM13920 internal circuit consumption when none of the SRCx provides enough power or when the battery is fully charged. Thus, battery discharging is kept minimal. SLEEP STATE is also reached when charging is not allowed (temperature outside range, boost converters disabled, V_{SRCx} below the sleep threshold).

The following conditions are defined:

- SLEEP CONDITION is true if one of the following conditions is true:
  - Temperature outside of the range (see Section 9.6).
  - All boost converters are disabled through I²C (see Section 9.11.4).
  - Voltage on both SRCx is below the sleep threshold (see Section 9.11.9).
- SUPPLY CONDITION is true if all the following conditions are true:
  - Temperature within the range (see Section 9.6).
  - At least one boost converter is enabled (see Section 9.11.4).
  - Voltage on one of SRCx is above the sleep threshold (see Section 9.11.9).

In SLEEP STATE, the AEM13920 behaves as follows:

- The battery connected on STO is not charged by SRCx, allowing for reducing the quiescent current on VINT and thus on STO.

- If V_{STO} is below V_{OVCH}, the battery connected on STO can be charged from the 5V charger by connecting a power source on 5V_IN.
- The AEM13920 internal circuit connected on VINT is supplied by the battery regardless of the power available on SRCx or 5V_IN.
- The buck converter (LOAD) is enabled (if enabled by the user).
- ST_STO is HIGH.

When in SLEEP STATE, the AEM13920 switches back to SUPPLY STATE if one of the following conditions is met:

- SUPPLY CONDITION and $V_{STO} < V_{OVCH}$.
- $V_{STO} < V_{OVDIS}$.

9. System Configuration

9.1. Configuration Pins and I²C

9.1.1. Configuration Pins

After a cold start, the AEM13920 reads the configuration pins. Those are then read periodically every $T_{GPIO,MON}$. The configuration pins can be changed on-the-fly. The floating configuration pins are read as HIGH, except SHIP_MODE which is read as LOW.

9.1.2. Configuration by I²C

To configure the AEM13920 through the I²C interface after a cold start, user must wait for the IRQ pin to rise, showing that the AEM13920 is out of RESET STATE and is ready to communicate with I²C. Please note that the IRQ pin is always low during RESET STATE. See Section 8.6 for further informations about the IRQ pin.

Once the above procedure is done, user can then write to the desired registers and validate the configuration by setting the CTRL.UPDATE register field. All configuration pins are then ignored (except the SHIP_MODE pin) and all configurations are set by the register values. All registers have a default value, that can be found in Table 15.

Registers are stored in a volatile memory, so their value is lost when VINT drops below the reset voltage $V_{INT,RESET}$, making the AEM13920 switch to RESET STATE. VDDIO is only for I²C communication bus supply, so register values are kept whether VDDIO is supplied or not once resisters are written.

9.2. Maximum Power Point Tracking

The following configurations apply when SRCx_MODE is HIGH, so that the boost converter is in MPPT mode. When configuring the MPPT module, user can set the MPP ratio and the timings, as shown in Tables 9 and 10.

Configuration pins			MPPT Ratio [%]
SRCx_CFG[2:0]			R_{MPPT}
0	0	0	35%
0	0	1	50%
0	1	0	65%
0	1	1	70%
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	ZMPP (SRC1) / 100% (SRC2)

Table 9: MPPT ratio configuration with SRCx_CFG[2:0] pins

Configuration pins		Sampling Duration [ms]	Period [ms]
SRCx_CFG[4:3]		$T_{MPPT,SAMPLING}$	$T_{MPPT,PERIOD}$
0	0	2	128
0	1	8	512
1	0	32	2048
1	1	256	16384

Table 10: MPPT timing configuration with SRCx_CFG[4:3] pins

9.3. Source Voltage Regulation

The following configurations apply when SRCx_MODE is LOW, so that the boost converter is in constant voltage mode. User can set the regulation voltage with SRCx_CFG[4:0] (see Table 11), or through the SRCxREGUx registers (see Section 9.11.2).

Configuration pins					Voltage [V]
SRCx_CFG[4:0]					$V_{SRCx,REG}$
0	0	0	0	0	0.14
0	0	0	0	1	0.30
0	0	0	1	0	0.36
0	0	0	1	1	0.42
0	0	1	0	0	0.48
0	0	1	0	1	0.51
0	0	1	1	0	0.525
0	0	1	1	1	0.54
0	1	0	0	0	0.555
0	1	0	0	1	0.57
0	1	0	1	0	0.60
0	1	0	1	1	0.66
0	1	1	0	0	0.72
0	1	1	0	1	0.735
0	1	1	1	0	0.75
0	1	1	1	1	0.765

Configuration pins					Voltage [V]
SRCx_CFG[4:0]					$V_{SRCx,REG}$
1	0	0	0	0	0.78
1	0	0	0	1	0.81
1	0	0	1	0	0.87
1	0	0	1	1	0.93
1	0	1	0	0	0.99
1	0	1	0	1	1.10
1	0	1	1	0	1.20
1	0	1	1	1	1.31
1	1	0	0	0	1.40
1	1	0	0	1	1.50
1	1	0	1	0	1.61
1	1	0	1	1	1.70
1	1	1	0	0	1.79
1	1	1	0	1	1.90
1	1	1	1	0	1.99
1	1	1	1	1	2.10

Table 11: Configuration of the source constant regulation voltage with SRCx_CFG[4:0] pins

9.4. Storage Element Thresholds

The storage element protection thresholds V_{OVCH}, V_{CHRDY} and V_{OVCH}, can be configured through the STO_CFG[2:0] pins as shown in Table 12.

Configuration pins			Overdischarge voltage [V]	Charge ready voltage [V]	Overcharge voltage [V]	Battery Type
STO_CFG[2:0]			V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
0	0	0	2.50	2.55	3.80	Lithium-ion Super Capacitor (LiC)
0	0	1	2.50	2.55	3.50	Lithium-ion Super Capacitor 85 °C (LiC)
0	1	0	3.00	3.30	4.12	Lithium-ion
0	1	1	3.00	3.30	3.90	Lithium-ion (long life)
1	0	0	3.50	3.55	3.90	Lithium-ion (super long life)
1	0	1	3.00	3.30	4.12	Lithium Polymer (LiPo)
1	1	0	2.80	3.10	3.63	Lithium Iron Phosphate (LiFePO4)
1	1	1	2.60	2.80	3.80	Tadiran HLC1020

Table 12: Storage element configuration with STO_CFG[2:0] pins

9.5. Buck Converter

Table 13 shows how to configure the regulated voltage on LOAD output with the LOAD_CFG[2:0] pins.

Configuration pins			LOAD voltage [V]
LOAD_CFG[2:0]			V_{LOAD}
0	0	0	Buck disabled
0	0	1	0.6
0	1	0	0.9
0	1	1	1.2
1	0	0	1.5
1	0	1	1.8
1	1	0	2.2
1	1	1	2.5[1]

Table 13: Configuration of LOAD voltage with LOAD_CFG[2:0] pins

1. This configuration is only available if $V_{OVDIS} \geq 2.5$ V.

Please refer to Section 9.11.5 to configure the peak current of the buck converter inductor (I²C register).

9.6. Thermal Monitoring

Thermal monitoring is configured by applying the following equations to determine a temperature threshold value to be written in registers TEMPCOLDCH, TEMPHOTCH, TEMPCOLDDIS or TEMPHOTDIS:

$$THRES = \frac{256 \cdot R_{TH}(T)}{R_{TH}(T) + R_{DIV}}$$

$$R_{TH}(T) = R0 \cdot e^{B \cdot \left(\frac{1}{T} - \frac{1}{T_0}\right)}$$

$$T = \frac{B}{\ln\left(\frac{R_{TH}(T)}{R0}\right) + \frac{B}{T_0}}$$

- THRES is the unsigned 8-bit value to be written in the registers to set the temperature threshold to the temperature T [K].
- R0 [Ω] is the resistance of the NTC thermistor at ambient temperature T_0 = 298.15 K (25 °C).
- $R_{TH}(T)$ [Ω] is the resistance of the thermistor at temperature T [K].
- T_0 [K] = 298.15 K (25 °C)
- T [K] is the current ambient temperature of the circuit.
- B is the characteristic constant of the thermistor, allowing to determine the resistance of the thermistor for a given temperature.

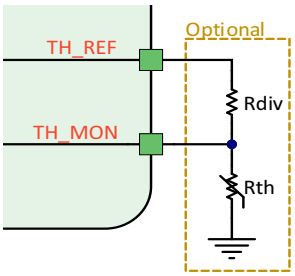


Figure 9: TH_REF and TH_MON connections

The typical values of R_{TH} and R_{DIV}, found in Table 7, allow for having a range of -25 °C to +70 °C for both charging and discharging.

Please note that the thermistor must be of the NTC (Negative Temperature Coefficient) type.

9.7. 5 V Charger

The 5 V charger implements CC/CV operation. When in CC, the maximum charging current $I_{5V,CC}$ can be set by connecting a resistor R_{5V_IMAX} between 5V_IMAX and GND:

$$I_{5V,CC} = \frac{50}{R_{5V\_MAX}}$$

Please note that R_{5V_IMAX} must be chosen so that $I_{5V,CC}$ complies with the range defined in Table 5. Example values can be found in Table 14:

Resistor [Ω]	Maximum Charging Current [mA]
R_{5V_IMAX}	$I_{5V,CC}$
370	135.0
680	73.5
1500	33.3
3700	13.5

Table 14: Typical resistor values for setting 5 V charger max. current

9.8. Shipping Mode

The shipping mode, described in Section 8.8, is enabled by connecting the SHIP_MODE pin to VINT and disabled by connecting the SHIP_MODE pin to GND or leaving it floating.

9.9. I²C Serial Interface Protocol

The AEM13920 uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (SDA) and a serial clock line (SCL). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

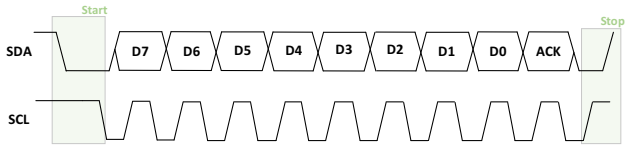


Figure 10: I²C transmission frame

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The AEM13920 is a slave that will receive configuration data or send the informations requested by the master.

The AEM13920 supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data are sent with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled-up (SDA and SCL are open drain outputs);
- Start bit (S): to initiates the transmission, the master switches the SDA line low while keeping SCL high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the SDA line from low to high while keeping SCL high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches SDA low;
- NACK: when the device receiving data keeps SDA high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x41 for the AEM13920.
- Bit [0] is the communication mode: 1 for 'read mode' (used when the master reads informations from the slave) and 0 for 'write mode' (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

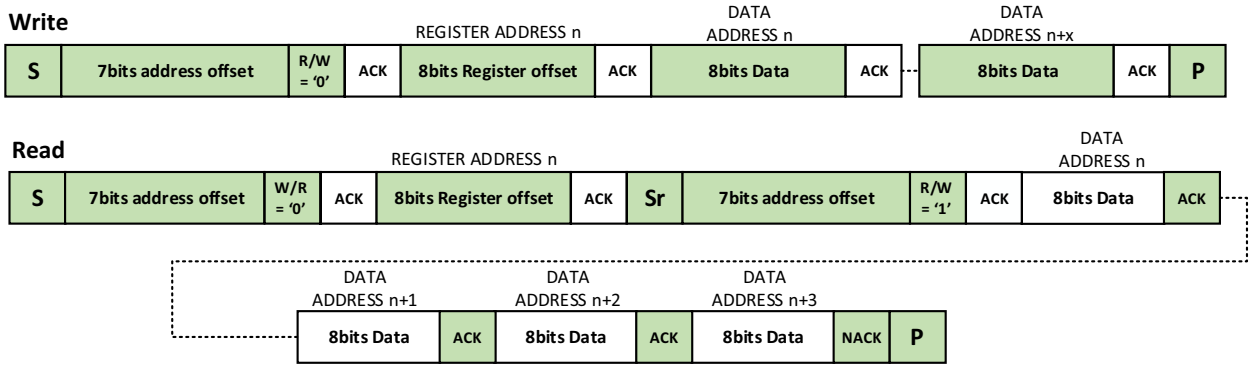
Here is the procedure for the master to write a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the TEMPCOLDCH register, the master sends the value 0x0B;
- Slave sends an ACK;
- Master sends the data to write to the register;
- Slave sends an ACK;
- If the master wants to write register at the next address (TEMPHOTCH in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several consecutive registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the APM0BUCK register, the master sends the value 0x1F;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in 'read' mode;
- Slave sends an ACK;
- Master provides the clock on SCL to allow the slave to shift the data of the read register on SDA;
- If the master wants to read register at the next address (APM1BUCK in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for writing several registers;
- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in Figure 11. Refer to Table 15 for all register addresses.



S = START
ACK = ACKNOWLEDGE
P = STOP
R/W = READ/WRITE
NACK = NOT ACKNOWLEGDE
Sr = RESTART

Figure 11: Read and write transmission

9.10. Register Map

Please note that the AEM13920 device address is 0x41.

Address	Name	Bit	Field Name	Access	Reset	Description
0x00	VERSION	[3:0]	MINOR	R	-	Minor revision number.
		[7:4]	MAJOR	R	-	Major revision number.
0x01	SRC1REGU0	[0:0]	MODE	R/W	0x01	SRC1 regulation mode.
		[3:1]	CFG0	R/W	0x00	SRC1 regulation mechanism configuration.
0x02	SRC1REGU1	[2:0]	CFG1	R/W	0x00	
		[5:3]	CFG2	R/W	0x00	
0x03	SRC2REGU0	[0:0]	MODE	R/W	0x01	SRC2 regulation mode.
		[3:1]	CFG0	R/W	0x00	SRC2 regulation mechanism configuration.
0x04	SRC2REGU1	[2:0]	CFG1	R/W	0x00	
		[5:3]	CFG2	R/W	0x00	
0x05	VOVDIS	[5:0]	THRESH	R/W	0x06	Storage element overdischarge threshold.
0x06	VCHRDY	[5:0]	THRESH	R/W	0x05	Storage element ready threshold.
0x07	VOVCH	[6:0]	THRESH	R/W	0x3A	Storage element overcharge threshold.
0x08	BST1CFG	[0:0]	EN	R/W	0x01	Boost SRC1 enable.
		[1:1]	HPEN	R/W	0x01	Boost SRC1 high-power mode enable.
		[4:2]	TMULT	R/W	0x01	Boost SRC1 current configuration.
0x09	BST2CFG	[0:0]	EN	R/W	0x01	Boost SRC2 enable.
		[1:1]	HPEN	R/W	0x01	Boost SRC2 high-power mode enable.
		[4:2]	TMULT	R/W	0x01	Boost SRC2 current configuration.
0x0A	BUCKCFG	[2:0]	VOUT	R/W	0x00	Buck voltage configuration.
		[5:3]	TMULT	R/W	0x03	Buck current configuration.
0x0B	TEMPCOLDCH	[7:0]	THRESH	R/W	0xD1	Cold temperature threshold for storage element charging.
0x0C	TEMPHOTCH	[7:0]	THRESH	R/W	0x18	Hot temperature threshold for storage element charging.
0x0D	TEMPCOLDDIS	[7:0]	THRESH	R/W	0xD1	Cold temperature threshold for storage element discharging.
0x0E	TEMPHOTDIS	[7:0]	THRESH	R/W	0x18	Hot temperature threshold for storage element discharging.
0x0F	TMON	[0:0]	EN	R/W	0x01	Temperature monitoring enable.
0x10	SLEEP	[2:0]	SRC1THRESH	R/W	0x00	Sleep threshold (SRC1).
		[5:3]	SRC2THRESH	R/W	0x00	Sleep threshold (SRC2).
0x11	APM	[0:0]	SRC1EN	R/W	0x00	APM SRC1 enable.
		[1:1]	SRC2EN	R/W	0x00	APM SRC2 enable.
		[2:2]	BUCKEN	R/W	0x00	APM LOAD enable.
		[3:3]	MODE	R/W	0x00	APM mode.
		[4:4]	WINDOW	R/W	0x00	APM computation window.

Table 15: Register map

Address	Name	Bit	Field Name	Access	Reset	Description
0x12	IRQEN0	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable.
		[1:1]	VOVDIS	R/W	0x00	IRQ VOVDIS enable.
		[2:2]	VCHRDY	R/W	0x00	IRQ VCHRDY enable.
		[3:3]	VOVCH	R/W	0x00	IRQ VOVCH enable.
		[4:4]	SLEEP	R/W	0x00	IRQ sleep threshold (SRCx) enable.
		[5:5]	TEMPCH	R/W	0x00	IRQ temperature (charge) enable.
		[6:6]	TEMPDIS	R/W	0x00	IRQ temperature (discharge) enable.
0x13	IRQEN1	[0:0]	SRC1MPPTSTART	R/W	0x00	IRQ MPPT start (SRC1) enable.
		[1:1]	SRC1MPPTDONE	R/W	0x00	IRQ MPPT done (SRC1) enable.
		[2:2]	SRC2MPPTSTART	R/W	0x00	IRQ MPPT start (SRC2) enable.
		[3:3]	SRC2MPPTDONE	R/W	0x00	IRQ MPPT done (SRC2) enable.
		[4:4]	STODONE	R/W	0x00	IRQ STO ADC done enable.
		[5:5]	TEMPDONE	R/W	0x00	IRQ temperature ADC done enable.
		[6:6]	APMDONE	R/W	0x00	IRQ APM done enable.
		[7:7]	APMERR	R/W	0x00	IRQ APM error enable.
0x14	CTRL	[0:0]	UPDATE	R/W	0x00	Load I²C registers configuration.
		[2:2]	SYNCBUSY	R/W	0x00	Synchronization busy flag.
0x15	IRQFLG0	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag.
		[1:1]	VOVDIS	R	0x00	IRQ VOVDIS flag.
		[2:2]	VCHRDY	R	0x00	IRQ VCHRDY flag.
		[3:3]	VOVCH	R	0x00	IRQ VOVCHH flag.
		[4:4]	SLEEP	R	0x00	IRQ sleep threshold (SRCx) flag.
		[5:5]	TEMPCH	R	0x00	IRQ temperature (charge) flag.
		[6:6]	TEMPDIS	R	0x00	IRQ temperature (discharge) flag.
0x16	IRQFLG1	[0:0]	SRC1MPPTSTART	R	0x00	IRQ MPPT start (SRC1) flag.
		[1:1]	SRC1MPPTDONE	R	0x00	IRQ MPPT done (SRC1) flag.
		[2:2]	SRC2MPPTSTART	R	0x00	IRQ MPPT start (SRC2) flag.
		[3:3]	SRC2MPPTDONE	R	0x00	IRQ MPPT done (SRC2) flag.
		[4:4]	STODONE	R	0x00	IRQ STO ADC done flag.
		[5:5]	TEMPDONE	R	0x00	IRQ temperature ADC done flag.
		[6:6]	APMDONE	R	0x00	IRQ APM done flag.
		[7:7]	APMERR	R	0x00	IRQ APM error flag.
0x17	STATUS0	[0:0]	VOVDIS	R	0x00	Status VOVIDS.
		[1:1]	VCHRDY	R	0x00	Status VCHRDY.
		[2:2]	VOVCH	R	0x00	Status VOVCH.
		[3:3]	SRC1SLEEP	R	0x00	Status sleep threshold (SRC1).
		[4:4]	SRC2SLEEP	R	0x00	Status sleep threshold (SRC2).
0x18	STATUS1	[0:0]	TEMPCOLDCH	R	0x00	Status cold temperature (charge).
		[1:1]	TEMPHOTCH	R	0x00	Status hot temperature (charge).
		[2:2]	TEMPCOLDDIS	R	0x00	Status cold temperature (discharge).
		[3:3]	TEMPHOTDIS	R	0x00	Status hot temperature (discharge).
0x19	APM0SRC1	[7:0]	DATA	R	0x00	APM data 0 (SRC1).
0x1A	APM1SRC1	[7:0]	DATA	R	0x00	APM data 1 (SRC1).
0x1B	APM2SRC1	[7:0]	DATA	R	0x00	APM data 2 (SRC1).

Table 15: Register map

Address	Name	Bit	Field Name	Access	Reset	Description
0x1C	APM0SRC2	[7:0]	DATA	R	0x00	APM data 0 (SRC2).
0x1D	APM1SRC2	[7:0]	DATA	R	0x00	APM data 1 (SRC2).
0x1E	APM2SRC2	[7:0]	DATA	R	0x00	APM data 2 (SRC2).
0x1F	APM0BUCK	[7:0]	DATA	R	0x00	APM data 0 (BUCK).
0x20	APM1BUCK	[7:0]	DATA	R	0x00	APM data 1 (BUCK).
0x21	APM2BUCK	[7:0]	DATA	R	0x00	APM data 2 (BUCK).
0x22	APMERR	[0:0]	SRC1OV	R	0x00	APM counter overflow SRC1.
		[1:1]	SRC1NVLD	R	0x00	APM counter corrupted SRC1.
		[2:2]	SRC2OV	R	0x00	APM counter overflow SRC2.
		[3:3]	SRC2NVLD	R	0x00	APM counter corrupted SRC2.
		[4:4]	BUCKOV	R	0x00	APM counter overflow BUCK.
		[5:5]	BUCKNVLD	R	0x00	APM counter corrupted BUCK.
0x23	TEMP	[7:0]	DATA	R	0x00	Temperature monitoring value.
0x24	STO	[7:0]	DATA	R	0x00	Storage monitoring value.
0x25	SRC1	[7:0]	DATA	R	0x00	SRC1 monitoring value.
0x26	SRC2	[7:0]	DATA	R	0x00	SRC2 monitoring value.

Table 15: Register map

9.11. Registers Configuration

9.11.1. Version Register (VERSION)

The VERSION register holds the version of the chip, with major and minor revision numbers.

VERSION Register	0x00	R
Bit [7:4]	Bit [3:0]	
MAJOR	MINOR	
0x00	0x00	

Table 16: VERSION Register

Bit [7:4]: major revision number (VERSION.MAJOR).

Bit [3:0]: minor revision number (VERSION.MINOR).

9.11.2. Source Regulation Configuration Registers (SRCxREGUx)

The SRCxREGUx registers allow for configuring SRCx regulation.

Table 17 shows the use of SRCxREGUx registers according to the source regulation mode.

- **SRCxREGU0.MODE = 0**: constant voltage regulation mode, as described in Section 9.11.2.3 and Table 20.
  - LVL [7:0] - Register value defining the constant regulation voltage.
- **SRCxREGU0.MODE = 1**: MPPT regulation mode, as described in Section 9.11.2.4 and in Tables 21, 22 and 23.
  - MPPT_RATIO [2:0] - Register value defining the MPPT ratio.
  - MPPT_SAMPLING [2:0] - Register value defining the MPPT sampling time.
  - MPPT_PERIOD [2:0] - Register value defining the MPPT period.

	SRCxREGU1								SRCxREGU0							
	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Register Field			CFG2			CFG1							CFG0			MODE
Mode 0 Constant Voltage				LVL[7:6]		LVL[5:3]							LVL [2:0]			MODE
Mode 1 MPPT			MPPT_PERDIOD [2:0]			MPPT_SAMPLING [2:0]							MPPT_RATIO [2:0]			MODE

Table 17: Summary of APMxSRCx register fields

9.11.2.1. SRCxREGU0

SRCxREGU0 are the first configuration registers for configuring SRCx regulation voltage mechanism.

Please note that, when SRCxREGU0 = 0, SRCxREGU1.CFG2 [2] (SRCxREGU1 [5]) is not used.

SRC1REGU0 Register **SRC2REGU0 Register**	**0x01** **0x03**	**R/W** **R/W**
Bit [7:4]	Bit [3:1]	Bit [0]
RESERVED	CFG0	MODE
0x00	0x00	1

Table 18: SRCxREGU0 Register

Bit [3:1]: SRCx configuration 0 (SRCxREGU0.CFG0).

This fields is used to configure SRCx regulation mechanism. Depending on MODE value, this fields is used to configure the following parameters:

- **MODE = 0:** SRCx regulation voltage, along with the other SRCxREGUx.CFGx registers fields.
- **MODE = 1:** ratio/ZMPP, as set by other SRCxREGUx.CFGx registers fields.

Bit [0]: SRCx regulation mode (SRCxREGU0.MODE).

This fields is used to configure SRCx regulation mode:

- 0: select regulation as constant voltage.
- 1: select regulation as MPPT (V_{MPP} / V_{OC} or ZMPP).

9.11.2.2. SRCxREGU1

SRCxREGU1 are the second configuration registers for configuring SRCx regulation voltage mechanism.

SRC1REGU1 Register SRC2REGU1 Register	0x02 0x04	R/W R/W
Bit [7:6]	Bit [5:3]	Bit [2:0]
RESERVED	CFG2	CFG1
0x00	0x00	0x00

Table 19: SRCxREGU1 Register

Bit [5:3]: SRCx configuration 2 (SRCxREGU1.CFG2).

This fields is used to configure SRCx regulation mechanism. Depending on MODE value, this fields is used to configure the following parameters:

- MODE = 0: SRCx regulation voltage, along with the other SRCxREGUx.CFGx registers fields.
- MODE = 1: SRCx MPPT sampling duration $T_{MPPT,SAMPLING}$.

Bit [2:0]: SRCx configuration 1 (SRCxREGU1.CFG1).

This fields is used to configure SRCx regulation mechanism. Depending on MODE value, this fields is used to configure the following parameters:

- MODE = 0: regulation voltage, along with the other SRCxREGUx.CFGx registers fields.
- MODE = 1: SRCx MPPT period $T_{MPPT,PERIOD}$.

9.11.2.3. Constant Voltage Configuration

Table 20 describes how to configure SRCxREGUx registers when the AEM13920 source regulation mode is set to constant voltage.

See Table 17 for a description of how LVL [7:0] is distributed across SRCxREGUx registers.

LVL [7:0]	$V_{SRCx,REG}$ [V]	LVL [7:0]	$V_{SRCx,REG}$ [V]	LVL [7:0]	$V_{SRCx,REG}$ [V]	LVL [7:0]	$V_{SRCx,REG}$ [V]	LVL [7:0]	$V_{SRCx,REG}$ [V]	LVL [7:0]	$V_{SRCx,REG}$ [V]
0x00	0.113	0x2A	0.375	0x4A	0.855	0x6A	1.335	0x8A	1.970	0xAA	3.182
...	...	0x2B	0.390	0x4B	0.870	0x6B	1.350	0x8B	1.993	0xAB	3.227
0x0C	0.113	0x2C	0.405	0x4C	0.885	0x6C	1.365	0x8C	2.015	0xAC	3.273
0x0D	0.120	0x2D	0.420	0x4D	0.900	0x6D	1.380	0x8D	2.037	0xAD	3.318
0x0E	0.128	0x2E	0.435	0x4E	0.915	0x6E	1.395	0x8E	2.060	0xAE	3.364
0x0F	0.135	0x2F	0.450	0x4F	0.930	0x6F	1.410	0x8F	2.082	0xAF	3.409
0x10	0.143	0x30	0.465	0x50	0.945	0x70	1.425	0x90	2.104	0xB0	3.455
0x11	0.150	0x31	0.480	0x51	0.960	0x71	1.440	0x91	2.127	0xB1	3.500
0x12	0.158	0x32	0.495	0x52	0.975	0x72	1.455	0x92	2.149	0xB2	3.545
0x13	0.165	0x33	0.510	0x53	0.990	0x73	1.470	0x93	2.172	0xB3	3.591
0x14	0.173	0x34	0.525	0x54	1.005	0x74	1.478	0x94	2.194	0xB4	3.636
0x15	0.180	0x35	0.540	0x55	1.020	0x75	1.500	0x95	2.227	0xB5	3.682
0x16	0.188	0x36	0.555	0x56	1.035	0x76	1.522	0x96	2.273	0xB6	3.727
0x17	0.195	0x37	0.570	0x57	1.050	0x77	1.545	0x97	2.318	0xB7	3.773
0x18	0.203	0x38	0.585	0x58	1.065	0x78	1.567	0x98	2.364	0xB8	3.818
0x19	0.210	0x39	0.600	0x59	1.080	0x79	1.590	0x99	2.409	0xB9	3.864
0x1A	0.218	0x3A	0.615	0x5A	1.095	0x7A	1.612	0x9A	2.455	0xBA	3.909
0x1B	0.225	0x3B	0.630	0x5B	1.110	0x7B	1.634	0x9B	2.500	0xBB	3.955
0x1C	0.233	0x3C	0.645	0x5C	1.125	0x7C	1.657	0x9C	2.545	0xBC	4.000
0x1D	0.240	0x3D	0.660	0x5D	1.140	0x7D	1.679	0x9D	2.591	0xBD	4.045
0x1E	0.248	0x3E	0.675	0x5E	1.155	0x7E	1.701	0x9E	2.636	0xBE	4.091
0x1F	0.255	0x3F	0.690	0x5F	1.170	0x7F	1.724	0x9F	2.682	0xBF	4.136
0x20	0.263	0x40	0.705	0x60	1.185	0x80	1.746	0xA0	2.727	0xC0	4.182
0x21	0.270	0x41	0.720	0x61	1.200	0x81	1.769	0xA1	2.773	0xC1	4.227
0x22	0.278	0x42	0.735	0x62	1.215	0x82	1.791	0xA2	2.818	0xC2	4.273
0x23	0.285	0x43	0.750	0x63	1.230	0x83	1.813	0xA3	2.864	0xC3	4.318
0x24	0.293	0x44	0.765	0x64	1.245	0x84	1.836	0xA4	2.909	0xC4	4.364
0x25	0.300	0x45	0.780	0x65	1.260	0x85	1.858	0xA5	2.955	0xC5	4.409
0x26	0.315	0x46	0.795	0x66	1.275	0x86	1.881	0xA6	3.000	0xC6	4.455
0x27	0.330	0x47	0.810	0x67	1.290	0x87	1.903	0xA7	3.045	...	...
0x28	0.345	0x48	0.825	0x68	1.305	0x88	1.925	0xA8	3.091		
0x29	0.360	0x49	0.840	0x69	1.320	0x89	1.948	0xA9	3.136	0xFF	4.455

Table 20: SRCx constant voltage values configured by SRCxREGUx (SRCxREGU0.MODE = 0)

9.11.2.4. MPPT Configuration

This section describes how to configure the MPPT module through the SRCxREGUx registers.

See Table 17 for the distribution of MPPT_RATIO [2:0], MPPT_SAMPLING [2:0], MPPT_PERIOD [2:0] values across SRCxREGUx registers.

- Table 21 shows the configuration of SRCxREGU0.CFG0 register field to set the MPPT ratio.
- Table 22 shows the configuration of SRCxREGU1.CFG1 register field to set the MPPT sampling duration.
- Table 23 shows the configuration of SRCxREGU1.CFG2 register field to set the MPPT period.

SRCxREGU0.CFG0 MPPT_RATIO [2:0]			R_{MPPT} / ZMPP
0	0	0	35 %
0	0	1	50 %
0	1	0	65 %
0	1	1	70 %
1	0	0	75 %
1	0	1	80 %
1	1	0	85 %
1	1	1	SRC1: ZMPP SRC2: 100 %

Table 21: SRCx MPPT ratio/ZMPP configured by SRCxREGUx (SRCxREGU0.MODE = 1)

SRCxREGU1.CFG1 MPPT_SAMPLING [2:0]			$T_{MPPT,SAMPLING}$ [ms]
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	128
1	1	0	256
1	1	1	512

Table 22: SRCx MPPT sampling duration configured by SRCxREGUx (SRCxREGU0.MODE = 1)

SRCxREGU1.CFG2 MPPT_PERIOD [2:0]			$T_{MPPT,PERIOD}$ [ms]
0	0	0	128
0	0	1	256
0	1	0	512
0	1	1	1024
1	0	0	2048
1	0	1	4096
1	1	0	8192
1	1	1	16384

Table 23: SRCx MPPT period configured by SRCxREGUx (SRCxREGU0.MODE = 1)

9.11.3. Storage Element Threshold Voltages (VOVDIS / VCHRDY / VOVCH)

The storage element protection thresholds, described in Section 9.4, can be set independently by the registers VOVDIS, VCHRDY and VOVCH.

9.11.3.1. Overdischarge Voltage (VOVDIS)

The VOVDIS register allows for configuring V_{OVDIS}, as shown in Table 25.

VOVDIS Register	0x05	R/W
Bit [7:6]	Bit [5:0]	
RESERVED	THRESH	
0x00	0x06	

Table 24: VOVDIS Register

VOVDIS [5:0]	V_{OVDIS} [V]	VOVDIS [5:0]	V_{OVDIS} [V]	VOVDIS [5:0]	V_{OVDIS} [V]	VOVDIS [5:0]	V_{OVDIS} [V]
0x00	2.400	0x10	2.700	0x20	3.000	0x30	3.300
0x01	2.419	0x11	2.719	0x21	3.019	0x31	3.319
0x02	2.438	0x12	2.738	0x22	3.038	0x32	3.338
0x03	2.456	0x13	2.756	0x23	3.056	0x33	3.356
0x04	2.475	0x14	2.775	0x24	3.075	0x34	3.375
0x05	2.494	0x15	2.794	0x25	3.094	0x35	3.394
0x06	2.513	0x16	2.813	0x26	3.113	0x36	3.413
0x07	2.531	0x17	2.831	0x27	3.131	0x37	3.431
0x08	2.550	0x18	2.850	0x28	3.150	0x38	3.450
0x09	2.569	0x19	2.869	0x29	3.169	0x39	3.469
0x0A	2.588	0x1A	2.888	0x2A	3.188	0x3A	3.488
0x0B	2.606	0x1B	2.906	0x2B	3.206	0x3B	3.506
0x0C	2.625	0x1C	2.925	0x2C	3.225	0x3C	3.525
0x0D	2.644	0x1D	2.944	0x2D	3.244	0x3D	3.544
0x0E	2.663	0x1E	2.963	0x2E	3.263	0x3E	3.563
0x0F	2.681	0x1F	2.981	0x2F	3.281	0x3F	3.581

Table 25: Storage element V_{OVDIS} configuration by VOVDIS register

9.11.3.2. Charge Ready Voltage (VCHRDY)

The VCHRDY register allows for configuring V_{CHRDY}, as shown in Table 27.

VCHRDY Register	0x06	R/W
Bit [7:6]	Bit [5:0]	
RESERVED	THRESH	
0x00	0x05	

Table 26: VCHRDY Register

VCHRDY [5:0]	V_{CHRDY} [V]	VCHRDY [5:0]	V_{CHRDY} [V]	VCHRDY [5:0]	V_{CHRDY} [V]	VCHRDY [5:0]	V_{CHRDY} [V]
0x00	2.456	0x10	2.756	0x20	3.056	0x30	3.356
0x01	2.475	0x11	2.775	0x21	3.075	0x31	3.375
0x02	2.494	0x12	2.794	0x22	3.094	0x32	3.394
0x03	2.512	0x13	2.812	0x23	3.112	0x33	3.412
0x04	2.531	0x14	2.831	0x24	3.131	0x34	3.431
0x05	2.550	0x15	2.850	0x25	3.150	0x35	3.450
0x06	2.569	0x16	2.869	0x26	3.169	0x36	3.469
0x07	2.587	0x17	2.887	0x27	3.187	0x37	3.487
0x08	2.606	0x18	2.906	0x28	3.206	0x38	3.506
0x09	2.625	0x19	2.925	0x29	3.225	0x39	3.525
0x0A	2.644	0x1A	2.944	0x2A	3.244	0x3A	3.544
0x0B	2.662	0x1B	2.962	0x2B	3.262	0x3B	3.562
0x0C	2.681	0x1C	2.981	0x2C	3.281	0x3C	3.581
0x0D	2.700	0x1D	3.000	0x2D	3.300	0x3D	3.600
0x0E	2.719	0x1E	3.019	0x2E	3.319	0x3E	3.619
0x0F	2.737	0x1F	3.037	0x2F	3.337	0x3F	3.637

Table 27: Storage element V_{CHRDY} configuration by VCHRDY register

9.11.3.3. Overcharge Voltage (VOVCH)

The VOVCH register allows for the configuration of V_{OVCH}, as shown in Table 29.

VOVCH Register	0x07	R/W
Bit [7]	Bit [6:0]	
RESERVED	THRESH	
0x00	0x3A	

Table 28: VOVCH Register

VOVCH	V_{OVCH} [V]	VOVCH	V_{OVCH} [V]	VOVCH	V_{OVCH} [V]	VOVCH	V_{OVCH} [V]
0x00	2.700	0x1B	3.206	0x36	3.713	0x51	4.219
0x01	2.719	0x1C	3.225	0x37	3.731	0x52	4.238
0x02	2.738	0x1D	3.244	0x38	3.750	0x53	4.256
0x03	2.756	0x1E	3.263	0x39	3.769	0x54	4.275
0x04	2.775	0x1F	3.281	0x3A	3.788	0x55	4.294
0x05	2.794	0x20	3.300	0x3B	3.806	0x56	4.313
0x06	2.813	0x21	3.319	0x3C	3.825	0x57	4.331
0x07	2.831	0x22	3.338	0x3D	3.844	0x58	4.350
0x08	2.850	0x23	3.356	0x3E	3.863	0x59	4.369
0x09	2.869	0x24	3.375	0x3F	3.881	0x5A	4.388
0x0A	2.888	0x25	3.394	0x40	3.900	0x5B	4.406
0x0B	2.906	0x26	3.413	0x41	3.919	0x5C	4.425
0x0C	2.925	0x27	3.431	0x42	3.938	0x5D	4.444
0x0D	2.944	0x28	3.450	0x43	3.956	0x5E	4.463
0x0E	2.963	0x29	3.469	0x44	3.975	0x5F	4.481
0x0F	2.981	0x2A	3.488	0x45	3.994	0x60	4.500
0x10	3.000	0x2B	3.506	0x46	4.013	0x61	4.519
0x11	3.019	0x2C	3.525	0x47	4.031	0x62	4.538
0x12	3.038	0x2D	3.544	0x48	4.050	0x63	4.556
0x13	3.056	0x2E	3.563	0x49	4.069	0x64	4.575
0x14	3.075	0x2F	3.581	0x4A	4.088	0x65	4.594
0x15	3.094	0x30	3.600	0x4B	4.106		
0x16	3.113	0x31	3.619	0x4C	4.125		
0x17	3.131	0x32	3.638	0x4D	4.144	...	...
0x18	3.150	0x33	3.656	0x4E	4.163		
0x19	3.169	0x34	3.675	0x4F	4.181		
0x1A	3.188	0x35	3.694	0x50	4.200	0x7F	4.594

Table 29: Storage element V_{OVCH} configuration by VOVCH register

9.11.4. Boost Converters (BSTxCFG)

The settings of the boost converters can be configured with registers BSTxCFG.

BST1CFG Register BST2CFG Register	0x08 0x09	R/W R/W	
Bit [7:5]	Bit [4:2]	Bit [1]	Bit [0]
RESERVED	TMULT	HPEN	EN
0x00	0x01	1	1

Table 30: BSTxCFG Registers

Bit [4:2]: boost converter timing configuration (TMULT)

This field allows for modifying the peak current of the boost inductor by increasing/decreasing the on/off timings of the boost converter. The higher the timing multiplier, the higher the boost inductor peak current, and thus the higher the average source current pulled from SRCx to STO.

The peak current in the inductor also depends on the value of the inductor.

TMULT	Timing Multiplier	Minimum L_{BOOSTx} Inductance [µH][1]
0x00	x1	4
0x01	x2	8
0x02	x3	12
0x03	x4	16
0x04	x6	24
0x05	x8	32
0x06	x12	48
0x07	x16	64

Table 31: Minimum buck inductor values according to buck timing

1. Never install an inductor which inductance is lower than those values for each setting of the timing multiplier. This would cause permanent damage to the AEM13920.

Bit [1]: boost converter high power mode enable (ENHP)

Setting this bit to 1 allows the AEM13920 to automatically enter high-power mode if needed, allowing for more power to be harvested from SRCx (see Section 8.2.4).

Setting this bit to 0 disables automatic high-power mode.

Bit [0]: enable boost converter (EN)

Setting this bit to 1 enables the corresponding boost converter. Setting it to 0 disables it.

9.11.5. Buck Converter (BUCKCFG)

This register allows for configuring the buck converter, which output is the LOAD pin.

BUCKCFG Register	0x0A	R/W
Bit [7:6]	Bit [5:3]	Bit [2:0]
RESERVED	TMULT	VOUT
0x00	0x03	0x00

Table 32: BUCKCFG Register

Bit [5:3]: buck converter timing configuration (TMULT)

This field allows for modifying the peak current of the buck inductor by increasing/decreasing the on/off timings of the buck converter. The higher the timing multiplier, the higher the buck inductor peak current, and thus the higher the average current pulled from STO to LOAD.

The peak current in the inductor depends also on the value of the inductor. Table 33 shows the minimum inductor value that can be used for each timing without damaging the AEM13920.

TMULT	Timing Multiplier	Minimum L_{BUCK} Inductance [µH][1]
0x00	x1	1.6
0x01	x2	3.3
0x02	x3	4.9
0x03	x4	6.5
0x04	x6	9.8
0x05	x8	13.1
0x06	x12	19.5
0x07	x16	26.0

Table 33: Minimum buck inductor values according to buck timing

1. Never install an inductor which inductance is lower than those values for each setting of the timing multiplier. This would cause permanent damage to the AEM13920.

Bit [2:0]: buck converter output regulation voltage (VOUT)

This field allows for setting the regulation output voltage V_{LOAD} of the buck converter (supplying the LOAD pin). The available voltages can be found in Table 34. To switch off the buck converter, set BUCK.VOUT to 0x00.

BUCK.VOUT Register Value	V_{LOAD} [V]
0x00	OFF
0x01	0.6
0x02	0.9
0x03	1.2
0x04	1.5
0x05	1.8
0x06	2.2
0x07	2.5

Table 34: V_{LOAD} settings by BUCK.VOUT register.

9.11.6. STO Charge Temperature Monitoring (TEMPCOLDCH and TEMPHOTCH)

Those fields are used to configure the minimum (cold) and maximum (hot) temperature thresholds for charging the battery on STO.

THRESH value is determined as follows from the desired temperature T:

- Determine the resistance of the thermo resistor R_{TH} at the desired temperature.
- Calculate THRESH using the following formula:

$$THRESH = \frac{256 \cdot R_{TH}}{R_{DIV} + R_{TH}}$$

See Section 9.6 for further information about thermal monitoring configuration.

9.11.6.1. TEMPCOLDCH

Minimum temperature (cold) for storage element charging register.

TEMPCOLDCH Register	0x0B	R/W
Bit [7:0]		
THRESH		
0xD1		

Table 35: TEMPCOLDCH Register

Bit [7:0]: THRESH (TEMPCOLDCH.THRESH).

This fields is used to configure the minimum temperature (cold) threshold.

9.11.6.2. TEMPHOTCH

Maximum temperature (hot) for storage element charging register.

TEMPHOTCH Register	0x0C	R/W
Bit [7:0]		
THRESH		
0x18		

Table 36: TEMPHOTCH Register

Bit [7:0]: THRESH (TEMPHOTCH.THRESH).

This fields is used to configure the maximum temperature (hot) threshold.

9.11.7. STO Discharge Temperature Monitoring (TEMPCOLDDIS and TEMPHOTDIS)

Those fields are used to configure the minimum (cold) and maximum (hot) temperature thresholds for discharging the battery on STO.

See Section 9.6 for further information about thermal monitoring configuration.

9.11.7.1. TEMPCOLDDIS

Minimum temperature (cold) for storage element discharging register.

TEMPCOLDDIS Register	0x0D	R/W
Bit [7:0]		
THRESH		
0xD1		

Table 37: TEMPCOLDDIS Register

Bit [7:0]: THRESH (TEMPCOLDDIS.THRESH).

This fields is used to configure the minimum temperature (cold) threshold.

9.11.7.2. TEMPHOTDIS

Maximum temperature (hot) for storage element discharging register.

TEMPHOTDIS Register	0x0E	R/W
Bit [7:0]		
THRESH		
0x18		

Table 38: TEMPHOTDIS Register

Bit [7:0]: THRESH (TEMPHOTDIS.THRESH).

This fields is used to configure the maximum temperature (hot) threshold.

9.11.8. Temperature Monitoring Enable (TMON)

This register is used to enable/disable thermal monitoring described in Sections 9.11.6 and 9.11.7.

TMON Register	0x0F	R/W
Bit [7:1]		Bit [0]
RESERVED		EN
0x00		1

Table 39: TMON Register

Bit [0]: EN (TMON.EN).

This fields is used to enable the temperature monitoring:

- 0: DIS - Disable the temperature monitoring.
- 1: EN - Enable the temperature monitoring

9.11.9. Sleep Threshold (SLEEP)

Sleep V_{SRCx} threshold configuration register.

SLEEP Register	0x10	R/W
Bit [7:6]	Bit [5:3]	Bit [2:0]
RESERVED	SRC2THRESH	SRC1THRESH
0x00	0x00	0x00

Table 40: SLEEP Register

Bit [5:3]: SRC2THRESH (SLEEP.SRC2THRESH).

This field is used to configure the sleep threshold of SRC2.

Bit [2:0]: SRC1THRESH (SLEEP.SRC1THRESH).

This field is used to configure the sleep threshold of SRC1.

Table 41 shows the sleep threshold voltages $V_{SLEEP,THRESH}$ according to the configuration of SLEEP.SRCxTHRESH fields:

SRCxTHRESH	Sleep Voltage Threshold $V_{SLEEP,THRESH}$ [V]
0x00	0.112
0x01	0.202
0x02	0.255
0x03	0.300
0x04	0.360
0x05	0.405
0x06	0.510
0x07	0.600

Table 41: Sleep thresholds as configured by SLEEP register.

9.11.10. Average Power Monitoring (APM)

APM configuration register.

APM Register		0x11		R/W	
Bit [7:5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	WINDOW	MODE	BUCKEN	SRC2EN	SRC1EN
0x00	0	0	0	0	0

Table 42: APM Register

Bit [4]: WINDOW (APM.WINDOW).

This field is used to select the APM computation window.

- 0: 128MS - Select a computation window of 128 ms (64 ms if MPPT period is 128 ms).
- 1: 64MS - Select a computation window of 64 ms.

Bit [3]: MODE (APM.MODE).

This field is used to select the APM mode.

- 0: CNTR - Set the APM in counter mode.
- 1: PWR - Set the APM in power meter mode.

Bit [2]: BUCKEN (APM.BUCKEN).

This field is used to enable the APM for BUCK.

- 0: DIS - Disable the APM.
- 1: EN - Enable the APM.

Bit [1]: SRC2EN (APM.SRC2EN).

This field is used to enable the APM for SRC2.

- 0: DIS - Disable the APM.
- 1: EN - Enable the APM.

Bit [0]: SRC1EN (APM.SRC1EN).

This field is used to enable the APM for SRC1.

- 0: DIS - Disable the APM.
- 1: EN - Enable the APM.

9.11.11. IRQ Enable (IRQENx)

9.11.11.1. IRQEN0

Interrupts enable 0 register: configures on which event the IRQ pin is set HIGH, along with the IRQEN1 register.

IRQEN0 Register			0x12			R/W	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	TEMPDIS	TEMPCH	SLEEP	VOVCH	VCHRDY	VOVDIS	I2CRDY
0	0	0	0	0	0	0	1

Table 43: IRQEN0 Register

Bit [6]: TEMPDIS (IRQEN0.TEMPDIS).

Setting this bit enables or disables the generation of interrupts when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers).

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [5]: TEMPCH (IRQEN0.TEMPCH).

Setting this bit enables or disables the generation of interrupts when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers).

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [4]: SLEEP (IRQEN0.SLEEP).

Setting this bit enables or disables the generation of interrupts when both sources cross the sleep threshold (selected through the SLEEP.SRCxTHRESH fields).

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [3]: VOVCH (IRQEN0.VOVCH).

Setting this bit enables or disables the generation of interrupts when the storage element voltage crosses the overcharge threshold (selected through the VOVCH register).

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [2]: VCHRDY (IRQEN0.VCHRDY).

Setting this bit enables or disables the generation of interrupts when the storage element voltage crosses the ready threshold (selected through the VCHRDY register).

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [1]: VOVDIS (IRQEN0.VOVDIS).

Setting this bit enables or disables the generation of interrupts when the storage element voltage crosses the overdischarge threshold (selected through the VOVDIS register).

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [0]: I2CRDY (IRQEN0.I2CRDY).

Setting this bit enables or disables the generation of interrupts when the serial interface (I2C/AIC) is ready to communicate.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

9.11.11.2. IRQEN1

Interrupts enable 1 register: configures on which event the IRQ pin is set HIGH, along with the IRQEN0 register.

IRQEN1 Register				0x13		R/W	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
APMERR	APMDONE	TEMPDONE	STODONE	SRC2MPPTDONE	SRC2MPPTSTART	SRC1MPPTDONE	SRC1MPPTSTART
0	0	0	0	0	0	0	0

Table 44: IRQEN1 Register

Bit [7]: APMERR (IRQEN0.APMERR).

Setting this bit enables or disables the generation of interrupts when a APM (BUCK) error occurs.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [6]: APMDONE (IRQEN0.APMDONE).

Setting this bit enables or disables the generation of interrupts when new APM data are available.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [5]: TEMPDONE (IRQEN0.TEMPDONE).

Setting this bit enables or disables the generation of interrupts when the temperature ADC is done.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [4]: STODONE (IRQEN0.STODONE).

Setting this bit enables or disables the generation of interrupts when the STO ADC is done.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [3]: SRC2MPPTDONE (IRQEN0.SRC2MPPTDONE).

Setting this bit enables or disables the generation of interrupts when the MPPT (source 2) is done.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [2]: SRC2MPPTSTART (IRQEN0.SRC2MPPTSTART).

Setting this bit enables or disables the generation of interrupts when the MPPT (source 2) starts.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [1]: SRC1MPPTDONE (IRQEN0.SRC1MPPTDONE).

Setting this bit enables or disables the generation of interrupts when the MPPT (source 1) is done.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

Bit [0]: SRC1MPPTSTART (IRQEN0.SRC1MPPTSTART).

Setting this bit enables or disables the generation of interrupts when the MPPT (source 1) starts.

- 0: DIS - Disable the interrupt.
- 1: EN - Enable the interrupt.

9.11.12. IRQ Flags (IRQFLGx)

9.11.12.1. IRQFLG0

Interrupt flags 0 register.

IRQFLG0 Register				0x15		R	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	TEMPDIS	TEMPCH	SLEEP	VOVCH	VCHRDY	VOVDIS	I2CRDY
0	0	0	0	0	0	0	1

Table 45: IRQFLG0 Register

Bit [6]: TEMPDIS (IRQFLG0.TEMPDIS).

This interrupt flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element discharging (selected through the TEMPCOLDDIS and TEMPHOTDIS registers), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [5]: TEMPCH (IRQFLG0.TEMPCH).

This interrupt flag is set when the temperature crosses the minimum or maximum temperature allowed for storage element charging (selected through the TEMPCOLDCH and TEMPHOTCH registers), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [4]: SLEEP (IRQFLG0.SLEEP).

This interrupt flag is set when both sources cross the sleep threshold (selected through the SLEEP.SRCxTHRESH fields), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [3]: VOVCH (IRQFLG0.VOVCH).

This interrupt flag is set when the storage element voltage crosses the overcharge threshold (selected through the VOVCH register), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [2]: VCHRDY (IRQFLG0.VCHRDY).

This interrupt flag is set when the storage element voltage crosses the ready threshold (selected through the VCHRDY register), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [1]: VOVDIS (IRQFLG0.VOVDIS).

This interrupt flag is set when the storage element voltage crosses the overdischarge threshold (selected through the VOVDIS register), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [0]: I2CRDY (IRQFLG0.I2CRDY).

This interrupt flag is set when the serial interface (I2C/AIC) is ready to communicate, if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

9.11.12.2. IRQFLG1

Interrupt flags 1 register.

IRQFLG1 Register				0x16		R	
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
APMERR	APMDONE	TEMPDONE	STODONE	SRC2MPPTDONE	SRC2MPPTSTART	SRC1MPPTDONE	SRC1MPPTSTART
0	0	0	0	0	0	0	0

Table 46: XXX Register

Bit [7]: APMERR (IRQEN0.APMERR).

This interrupt flag is set when a APM (BUCK) error occurs, if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [6]: APMDONE (IRQEN0.APMDONE).

This interrupt flag is set when new APM data is available, if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [5]: TEMPDONE (IRQEN0.TEMPDONE).

This interrupt flag is set when the temperature ADC is done, if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [4]: STODONE (IRQEN0.STODONE).

This interrupt flag is set when the STO ADC is done, if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [3]: SRC2MPPTDONE (IRQEN0.SRC2MPPTDONE).

This interrupt flag is set when the MPPT is done (source 2), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [2]: SRC2MPPTSTART (IRQEN0.SRC2MPPTSTART).

This interrupt flag is set when the MPPT starts (source 2), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [1]: SRC1MPPTDONE (IRQEN0.SRC1MPPTDONE).

This interrupt flag is set when the MPPT is done (source 1), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

Bit [0]: SRC1MPPTSTART (IRQEN0.SRC1MPPTSTART).

This interrupt flag is set when the MPPT starts (source 1), if the corresponding interrupt source has been previously enabled.

- 0: NFLG - No interrupt flag raised.
- 1: FLG - Interrupt flag raised.

9.11.13. I²C Control (CTRL)

Control register.

CTRL Register	0x14		R/W
Bit [7:3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	SYNCBUSY	RESERVED	UPDATE
0x00	0	0	0

Table 47: CTRL Register

Bit [2]: SYNCBUSY (CTRL.SYNCBUSY).

This field indicates whether the synchronization from the I2C registers to the system registers is ongoing or not.

- 0: NSYNC - R: CTRL register not synchronizing.
- 1: SYNC - R: CTRL register synchronizing.

Bit [0]: UPDATE (CTRL.UPDATE).

This field is used to update all the I2C registers to the system registers and to control the source of the configuration (GPIO or I2C).

- 0: GPIO
  - W: triggers loading configurations from the GPIO.
  - R: configurations from the GPIO is currently used if read as 0.
- 1: I2C
  - W: triggers loading configurations from the I2C.
  - R: configurations from the I2C is currently used if read as 1.

9.11.14. Status (STATUSx)

9.11.14.1. STATUS0

Status 0 register.

STATUS0 Register	0x17			R	
Bit [7:5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	SRC2SLEEP	SRC1SLEEP	VOVCH	VCHRDY	VOVDIS
0x00	0	0	0	0	0

Table 48: STATUS0 Register

Bit [4]: SRC2SLEEP (STATUS0.SRC2SLEEP).

This status indicates whether the source is higher than the sleep level or not.

- 0: HIGH - The source is higher than the sleep level
- 1: LOW - The source is lower than the sleep level

Bit [3]: SRC1SLEEP (STATUS0.SRC1SLEEP).

This status indicates whether the source is higher than the sleep level or not.

- 0: HIGH - The source is higher than the sleep level
- 1: LOW - The source is lower than the sleep level

Bit [2]: VOVCH (STATUS0.VOVCH).

This status indicates whether the storage element voltage is higher than the overcharge level or not.

- 0: LOW - The storage element voltage is lower than the overcharge level
- 1: HIGH - The storage element voltage is higher than the overcharge level

Bit [1]: VCHRDY (STATUS0.VCHRDY).

This status indicates whether the storage element voltage is higher than the ready level or not.

- 0: LOW - The storage element voltage is lower than the ready level
- 1: HIGH - The storage element voltage is higher than the ready level

Bit [0]: VOVDIS (STATUS0.VOVDIS).

This status indicates whether the storage element voltage is higher than the overdischarge level or not.

- 0: LOW - The storage element voltage is higher than the overdischarge level
- 1: HIGH - The storage element voltage is lower than the overdischarge level

9.11.14.2. STATUS1

Status 1 register.

STATUS1 Register	0x18		R	
Bit [7:4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	TEMPHOTDIS	TEMPCOLDDIS	TEMPHOTCH	TEMPCOLDCH
0x00	0	0	0	0

Table 49: STATUS1 Register

Bit [3]: TEMPHOTDIS (STATUS1.TEMPHOTDIS).

This status indicates whether the temperature is higher than the hot threshold (for storage element discharging) or not.

- 0: LOW - The temperature is below the hot threshold.
- 1: HIGH - The temperature is above the hot threshold.

Bit [2]: TEMPCOLDDIS (STATUS1.TEMPCOLDDIS).

This status indicates whether the temperature is higher than the cold threshold (for storage element discharging) or not.

- 0: HIGH - The temperature is above the cold threshold.
- 1: LOW - The temperature is below the cold threshold.

Bit [1]: TEMPHOTCH (STATUS1.TEMPHOTCH).

This status indicates whether the temperature is higher than the hot threshold (for storage element charging) or not.

- 0: LOW - The temperature is below the hot threshold
- 1: HIGH - The temperature is above the hot threshold

Bit [0]: TEMPCOLDCH (STATUS1.TEMPCOLDCH).

This status indicates whether the temperature is higher than the cold threshold (for storage element charging) or not.

- 0: HIGH - The temperature is above the cold threshold
- 1: LOW - The temperature is below the cold threshold

9.11.15. APM Data Summary (APMxSRCx and APMxBUCK)

The APM data registers for both boost converters and for the buck converter all share the same field structure, as described in Table 50.

- **Pulse Counter Mode**: in that mode, the value in the APM data registers is the number of pulses drawn by the DCDC converter during the computation window (see Section 8.5). This value can be accessed directly in the COUNTER fields as shown in Table 50.
- **Power Meter mode**: in that mode, the value in the APM data registers is the energy value E_{APM} in nano-Joule. It can be read by left bit-shifting (OFFSET bits) the value in the POWER field and multiplying the result by the corresponding α parameter (see Table 51) and by the inductance of the DCDC converter L_{DCDC}.

$$E_{APM} = (POWER \ll OFFSET) \cdot \alpha \cdot L_{DCDC} \cdot T_{MULT}$$

	APM2SRCx APM2BUCK								APM1SRCx APM1BUCK								APM0SRCx APM0BUCK							
	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Register Field		APM2SRCx.DATA[6:0] APM2BUCK.DATA[6:0]							APM1SRCx.DATA[7:0] APM1BUCK.DATA[7:0]								APM0SRCx.DATA[7:0] APM0BUCK.DATA[7:0]							
Global APM Field		APM DATA [22:0]																						
Pulse Counter Mode			COUNTER [21:16]						COUNTER [15:8]								COUNTER [7:0]							
Power Meter Mode		OFFSET [3:0]				POWER [18:16]			POWER [15:8]								POWER [7:0]							

Table 50: Summary of APMxSRCx and APMxBUCK register fields

DCDC Converter	α
SRC1 Boost	TBD
SRC2 Boost	TBD
	TBD
LOAD Buck	TBD
	TBD
	TBD

Table 51: APM α parameter

9.11.16. SRCx APM Data (APMxSRCx)

9.11.16.1. APM0SRCx

APM data 0 register (SRCx).

APM0SRC1 Register	0x19	R
APM0SRC2 Register	0x1C	R
Bit [7:0]		
DATA		
0x00		

Table 52: APM0SRCx Register

Bit [7:0]: DATA (APM0SRCx.DATA).

This register contains the bits [7:0] of the SRCx APM data (see Table 50 for detailed fields according to APM mode).

9.11.16.2. APM1SRCx

APM data 1 register (SRCx).

APM1SRC1 Register	0x1A	R
APM1SRC2 Register	0x1D	R
Bit [7:0]		
DATA		
0x00		

Table 53: APM1SRCx Register

Bit [7:0]: DATA (APM1SRCx.DATA).

This register contains the bits [15:8] of the SRCx APM data (see Table 50 for detailed fields according to APM mode).

9.11.16.3. APM2SRCx

APM data 2 register (SRCx).

APM2SRC1 Register	0x1B	R
APM2SRC2 Register	0x1E	R
Bit [7]	Bit [6:0]	
RESERVED	DATA	
0	0x00	

Table 54: APM2SRCx Register (pulse counter mode)

Bit [6:0]: DATA (APM2SRCx.DATA).

This register contains the bits [22:16] of the SRCx APM data (see Table 50 for detailed fields according to APM mode).

9.11.17. BUCK APM Data (APMxBUCK)

9.11.17.1. APM0BUCK

APM data 0 register (BUCK).

APM0BUCK Register	0x1F	R
Bit [7:0]		
DATA		
0x00		

Table 55: APM0BUCK Register

Bit [7:0]: DATA (APM0BUCK.DATA).

This register contains the bits [7:0] of the BUCK APM data (see Table 50 for detailed fields according to APM mode).

9.11.17.2. APM1BUCK

APM data 1 register (BUCK).

APM1BUCK Register	0x20	R
Bit [7:0]		
DATA		
0x00		

Table 56: APM1BUCK Register

Bit [7:0]: DATA (APM1BUCK.DATA).

This register contains the bits [15:8] of the BUCK APM data (see Table 50 for detailed fields according to APM mode).

9.11.17.3. APM2BUCK

APM data 2 register (BUCK).

APM2BUCK Register	0x21	R
Bit [7]	Bit [6:0]	
RESERVED	DATA	
0	0x00	

Table 57: APM2BUCK Register (pulse counter mode)

Bit [6:0]: DATA (APM2BUCK.DATA).

This register contains the bits [22:16] of the BUCK APM data (see Table 50 for detailed fields according to APM mode).

9.11.18. APM Error (APMERR)

APM errors status register.

APMERR Register	0x22				R	
Bit [7:6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
RESERVED	BUCKNVLD	BUCKOV	SRC2NVLD	SRC2OV	SRC1NVLD	SRC1OV
0x00	0	0	0	0	0	0

Table 58: APMERR Register

Bit [5]: BUCKNVLD (APMERR.BUCKNVLD).

This field indicates whether the BUCK counter is corrupted or not, which occurs when BUCK runs in “bang-bang” controlled converter mode, when:

$$V_{STO} - V_{LOAD} < 0.25V$$

This field can be set both in pulse counter mode and in power meter mode.

- 0: OK - The BUCK counter is valid.
- 1: ERR - The BUCK counter is corrupted.

Bit [4]: BUCKOV (APMERR.BUCKOV).

This field indicates whether a counter overflow (BUCK) error occurred or not.

- 0: OK - No counter overflow (BUCK) error occurred.
- 1: ERR - A counter overflow (BUCK) error occurred

Bit [3]: SRC2NVLD (APMERR.SRC2NVLD).

This field indicates whether the SRC2 counter is corrupted or not, occurs when $V_{SRC2} > V_{STO}$ and BOOST runs in diode conduction mode. This field is never set if the APM is configured in pulses counter mode.

- 0: OK - The SRC2 counter is valid.
- 1: ERR - The SRC2 counter is corrupted.

Bit [2]: SRC2OV (APMERR.SRC2OV).

This field indicates whether a counter overflow (SRC2) error occurred or not.

- 0: OK - No counter overflow (SRC2) error occurred.
- 1: ERR - A counter overflow (SRC2) error occurred.

Bit [1]: SRC1NVLD (APMERR.SRC1NVLD).

This field indicates whether the SRC1 counter is corrupted or not, occurs when $V_{SRC1} > V_{STO}$ and BOOST runs in diode conduction. This field is never set if the APM is configured in pulses counter mode.

- 0: OK - The SRC1 counter is valid
- 1: ERR - The SRC1 counter is corrupted

Bit [0]: SRC1OV (APMERR.SRC1OV).

This field indicates whether a counter overflow (SRC1) error occurred or not.

- 0: OK - No counter overflow (SRC1) error occurred
- 1: ERR - A counter overflow (SRC1) error occurred

9.11.19. Temperature Monitoring Data (TEMP)

Temperature monitoring data register.

TEMP Register	0x23	R
Bit [7:0]		
DATA		
0x00		

Table 59: TEMP Register

Bit [7:0]: DATA (TEMP.DATA).

This field gives the code that results from the ADC acquisition for the temperature monitoring.

R_{TH} can be determined using the following equation:

$$R_{TH} = \frac{R_{DIV} \cdot DATA}{256 - DATA}$$

Thus the temperature T in Kelvin can be obtained with the following formula.

$$T = \frac{B}{\ln\left(\frac{R_{TH}}{R0}\right) + \frac{B}{T_0}}$$

See Section 8.4 for further information.

9.11.20. Storage Element Voltage Data (STO)

Storage monitoring register.

STO Register	0x24	R
Bit [7:0]		
DATA		
0x00		

Table 60: STO Register

Bit [7:0]: DATA (STO.DATA).

This field contains the code that results from the ADC acquisition for the storage monitoring. V_{STO} can be determined using the following formula:

$$V_{STO} = \frac{4.8 \cdot DATA}{256}$$

9.11.21. Sources Voltage Data (SRCx)

Source data registers (SRC1 and SRC2).

To convert data from the register to Volts, use either the formulas from Table 62 or the values from Table 63 used as a lookup table. Please note that values in register SRCx.DATA are always within the ranges given in those two tables.

SRC1 Register	0x25	R
SRC2 Register	0x26	R
Bit [7:0]		
DATA		
0x00		

Table 61: SRCx Register

Bit [7:0]: DATA (SRCx.DATA).

This field contains the code that results from the ADC acquisition for the MPPT regulation. Maximum value is 0xB9.

SRCx.DATA Range	Formula [V]
0x00 - 0x06	0.112
0x07 - 0x12	$0.09 + (2 \cdot DATA - 9) \cdot 0.0075$
0x13 - 0x39	$0.3 + (2 \cdot DATA - 37) \cdot 0.015$
0x6A - 0x79	$\frac{0.3 + (2 \cdot DATA - 165) \cdot 0.015}{0.67}$
0xA1 - 0xB9	$\frac{0.3 + (2 \cdot DATA - 293) \cdot 0.015}{0.33}$

Table 62: Source voltage V_{SRCx} from SRCx.DATA register value (formula)

SRCx.DATA [7:0]	V_{SRCx} [V]	SRCx.DATA [7:0]	V_{SRCx} [V]	SRCx.DATA [7:0]	V_{SRCx} [V]	SRCx.DATA [7:0]	V_{SRCx} [V]
0x00	0.112	0x1C	0.585	0x34	1.305	0xA3	2.409
...	...	0x1D	0.615	0x35	1.335	0xA4	2.500
0x06	0.112	0x1E	0.645	0x36	1.365	0xA5	2.591
0x07	0.128	0x1F	0.675	0x37	1.395	0xA6	2.682
0x08	0.143	0x20	0.705	0x38	1.425	0xA7	2.773
0x09	0.158	0x21	0.735	0x39	1.455	0xA8	2.864
0x0A	0.173	0x22	0.765	0x6A	1.500	0xA9	2.955
0x0B	0.188	0x23	0.795	0x6B	1.545	0xAA	3.045
0x0C	0.203	0x24	0.825	0x6C	1.590	0xAB	3.136
0x0D	0.218	0x25	0.855	0x6D	1.634	0xAC	3.227
0x0E	0.233	0x26	0.885	0x6E	1.679	0xAD	3.318
0x0F	0.248	0x27	0.915	0x6F	1.724	0xAE	3.409
0x10	0.263	0x28	0.945	0x70	1.769	0xAF	3.500
0x11	0.278	0x29	0.975	0x71	1.813	0xB0	3.591
0x12	0.293	0x2A	1.005	0x72	1.858	0xB1	3.682
0x13	0.315	0x2B	1.035	0x73	1.903	0xB2	3.773
0x14	0.345	0x2C	1.065	0x74	1.948	0xB3	3.864
0x15	0.375	0x2D	1.095	0x75	1.993	0xB4	3.955
0x16	0.405	0x2E	1.125	0x76	2.037	0xB5	4.045
0x17	0.435	0x2F	1.155	0x77	2.082	0xB6	4.136
0x18	0.465	0x30	1.185	0x78	2.127	0xB7	4.227
0x19	0.495	0x31	1.215	0x79	2.172	0xB8	4.318
0x1A	0.525	0x32	1.245	0xA1	2.227	0xB9	4.409
0x1B	0.555	0x33	1.275	0xA2	2.318		

Table 63: Source voltage V_{SRCx} from SRCx.DATA register value (lookup table)

10. Typical Application Circuits

10.1. Example Circuit 1

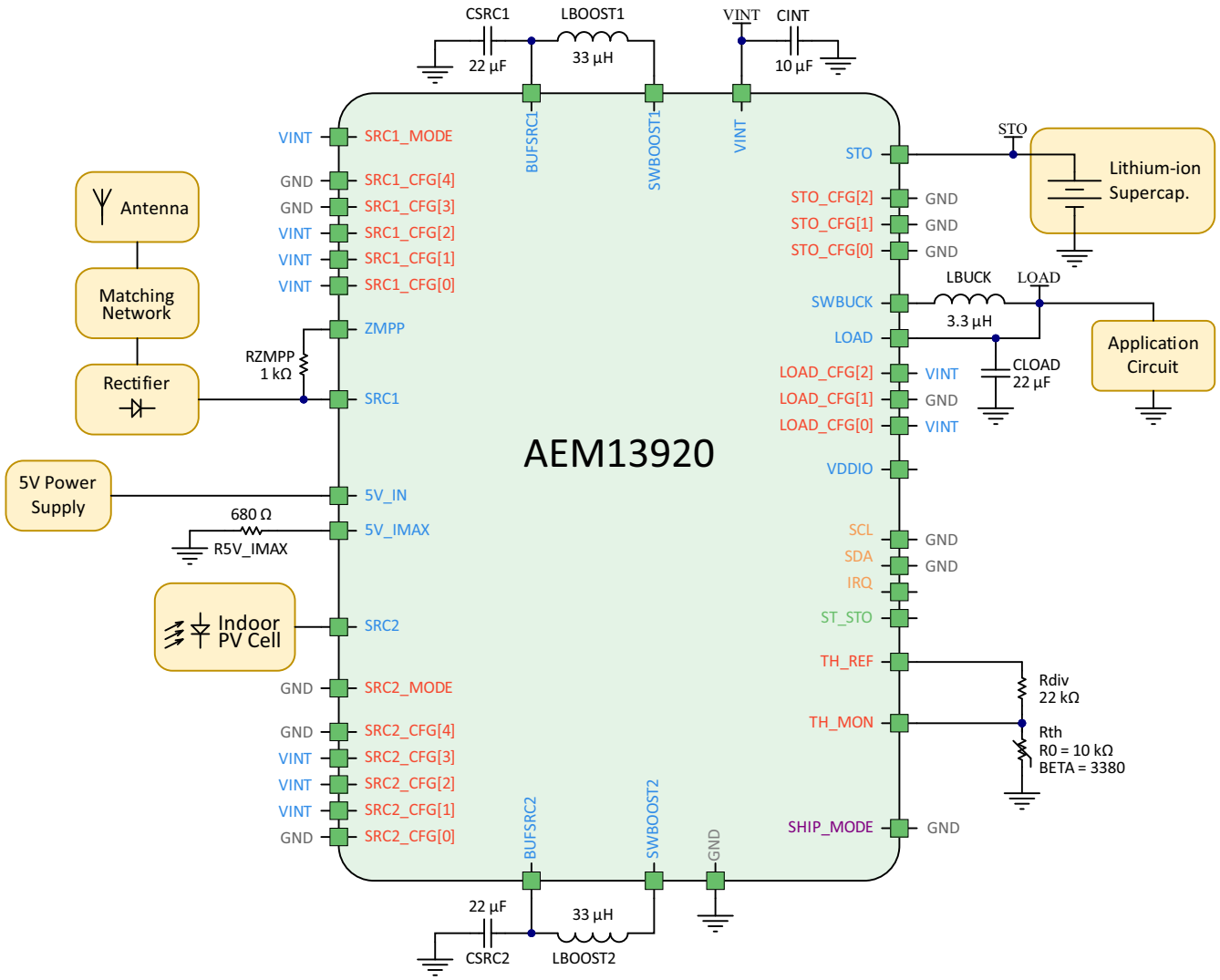


Figure 12: Typical application circuit 1

Figure 12 shows a typical application circuit of the AEM13920.

Configuration of SRC1

The first energy source is a RF harvester (antenna, matching network and RF rectifier), which has been optimized to provide maximum power when loaded with 1 kΩ. The fastest sampling/period is set to ensure maximum reactivity, as RF signal level is likely to change quickly.

- SRC1_MODE = H (MPPT).
- SRC1_CFG[2:0] = HHH (ZMPP mode).
- SRC1_CFG[4:3] = LL.
  - $T_{MPPT,SAMPLING}$ = 2 ms.
  - $T_{MPPT,PERIOD}$ = 128 ms.
- R_{ZMPP} = 1kΩ.
- L_{BOOST1} = 33 µH for best efficiency with default boost timing (see Section 9.11.4).

Configuration of SRC2

The second energy source is an indoor PV cell which has a constant 0.75 V MPP voltage. SRC2 is thus configured as follows:

- SRC2_MODE = L (constant voltage).
- SRC2_CFG[4:0] = LHHHL (0.75 V regulation).
- L_{BOOST2} = 33 µH for best efficiency with default boost timing (see Section 9.11.4).

Configuration of STO

The storage element is a Lithium-ion supercapacitor, so storage element threshold voltages are set as follows:

- STO_CFG[2:0] = LLL.
  - V_{OVDIS} = 2.50 V.
  - V_{CHRDY} = 2.55 V.
  - V_{OVCH} = 3.80 V.

Configuration of LOAD

The application circuit is supplied with 1.8 V with current peaks up to 100 mA. The buck converter is configured as follows:

- LOAD_CFG[2:0] = HLH (1.8 V)
- L_{BUCK} = 3.3 µH for high current capability.

Configuration of 5V_IN

The maximum allowed current to charge the storage element is 75 mA. Closest standard series resistor is 680 Ω, which leads to a 73.5 mA maximum current.

- R_{5V_IMAX} = 680 Ω.
- $I_{5V,CC}$ = 73.5 mA.

I²C configuration

I²C is not used:

- SDA and SCL are tied to GND.
- IRQ and VDDIO are left floating.

Temperature monitoring

Temperature monitoring is used to protect the storage element from being charged and discharged when temperature is outside the -25°C to +70°C range:

- R_{TH}:
  - R0 = 10 kΩ.
  - BETA = 3380.
- R_{DIV} = 22 kΩ.

Shipping mode

Shipping mode is not used.

- SHIP_MODE is connected to GND.

10.2. Example Circuit 2

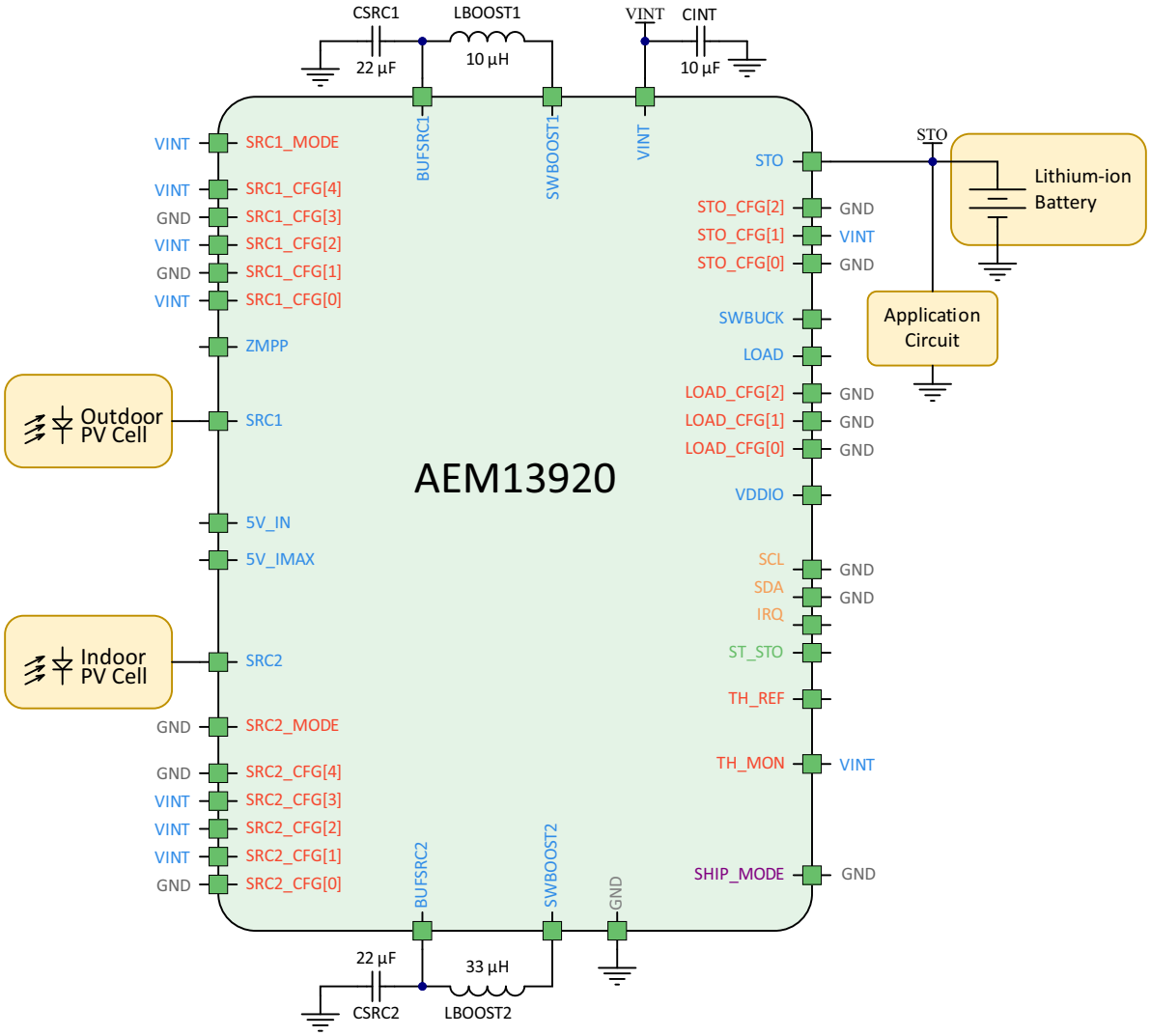


Figure 13: Typical application circuit 2

Figure 13 shows a typical application circuit of the AEM13920.

Configuration of SRC1

The first energy source is an outdoor PV cell. The MPPT is used with a 80% ratio. A medium sampling/period is set to ensure that the PV cell has enough time to reach its open circuit voltage during the V_{OC} sampling phase while still keeping a good reactivity to lighting changes.

- SRC1_MODE = H (MPPT).
- SRC1_CFG[2:0] = HLH (80%).
- SRC1_CFG[4:3] = LH.
  - $T_{MPPT,SAMPLING}$ = 32 ms.
  - $T_{MPPT,PERIOD}$ = 2048 ms.
- L_{BOOST1} = 10 µH for best efficiency/maximum current combination with default boost timing (see Section 9.11.4).

Configuration of SRC2

The second energy source is an indoor PV cell which has a constant 0.75 V maximum power point voltage. SRC2 is thus configured as follows:

- SRC2_MODE = L (constant voltage).
- SRC2_CFG[4:0] = LHHHL (0.75 V regulation).
- L_{BOOST2} = 33 µH for best efficiency with default boost timing (see Section 9.11.4).

Configuration of STO

The storage element is a Lithium-ion battery, so storage element threshold voltages are set as follows:

- STO_CFG[2:0] = LHL.
  - V_{OVDIS} = 3.00 V.
  - V_{CHRDY} = 3.30 V.
  - V_{OVCH} = 4.12 V.

Configuration of LOAD

The application circuit is supplied from the storage element, so the LOAD output is not used:

- LOAD_CFG[2:0] = LLL: buck converter is disabled.
- SWBUCK and LOAD are left floating.

Configuration of 5V_IN

The 5 V charger is not used:

- 5V_IN and 5V_IMAX are left floating.

I²C configuration

I²C is not used:

- SDA and SCL are tied to GND.
- IRQ and VDDIO are left floating.

Temperature monitoring

Temperature monitoring is not used:

- TH_MON is connected to VINT.
- TH_REF is left floating.

Shipping mode

Shipping mode is not used.

- SHIP_MODE is connected to GND.

10.3. Example Circuit 3

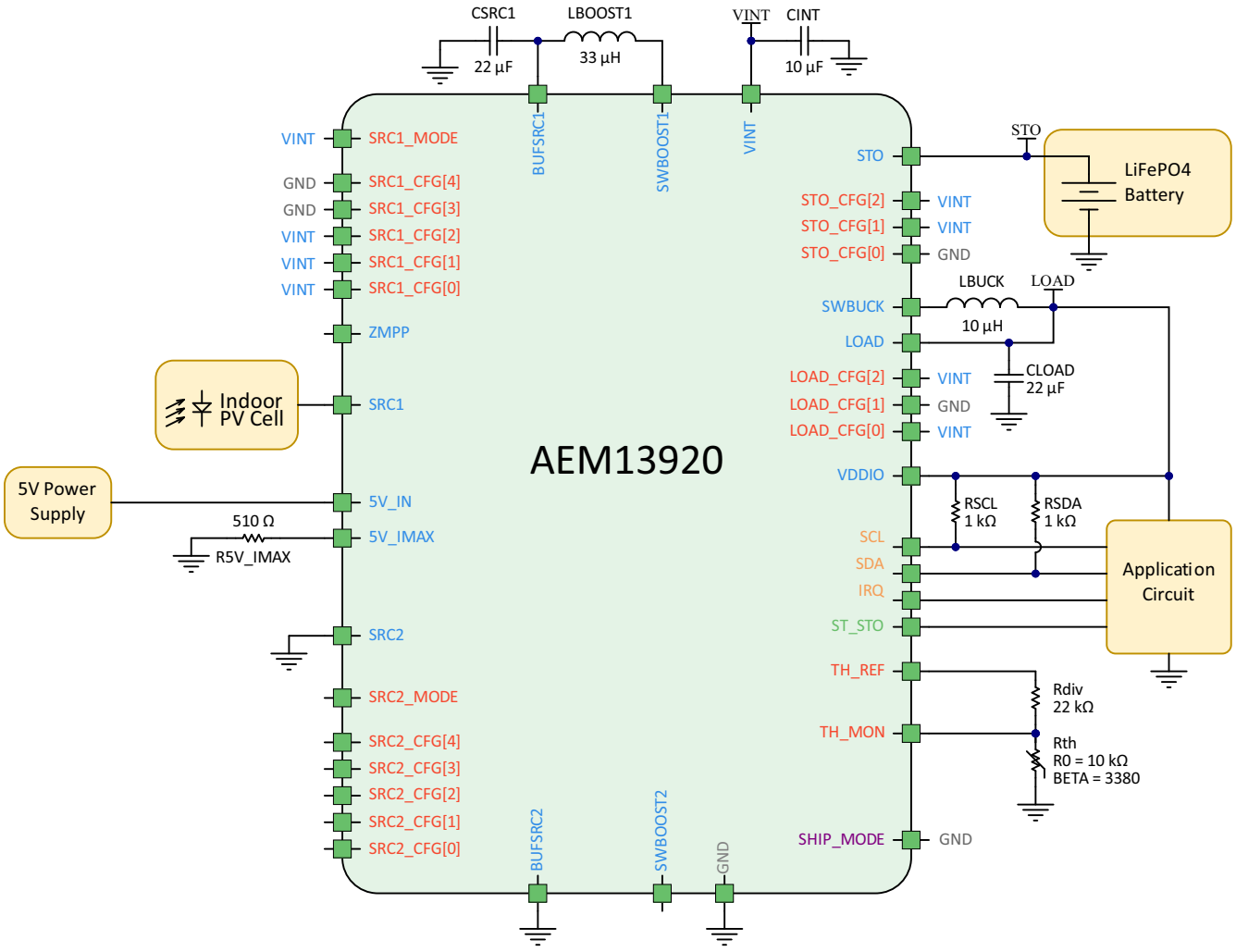


Figure 14: Typical application circuit 3

Figure 14 shows a typical application circuit of the AEM13920.

Configuration of SRC1

The energy source is an indoor PV cell which has a constant 0.60 V maximum power point voltage. SRC1 is thus configured as follows:

- SRC1_MODE = L (constant voltage).
- SRC1_CFG[4:0] = LHLHL (0.60 V regulation).
- L_{BOOST2} = 33 µH for best efficiency with default boost timing (see Section 9.11.4).

Configuration of SRC1

SRC2 boost converter is not used.

- SRC2, BUFSRC2 are connected to GND
- SWBOOST2 is left floating.
- SRC2_MODE and SRC2_CFG[4:0] are left floating.

Configuration of STO

The storage element is a $LiFePO_4$ battery, so storage element threshold voltages are set as follows:

- STO_CFG[2:0] = HHL.
  - V_{OVDIS} = 2.80 V.
  - V_{CHRDY} = 3.10 V.
  - V_{OVCH} = 3.63 V.

Configuration of LOAD

The application circuit is supplied with 1.8 V with current peaks up to 20 mA. The buck converter is configured as follows:

- LOAD_CFG[2:0] = HHH (2.5 V)
- L_{BUCK} = 10 µH for best efficiency.
- T_{MULT} = 2 for best efficiency at moderate current loads (configured through I²C register, see Table 64).

Configuration of 5V_IN

The maximum allowed current to charge the storage element is 100 mA. Closest standard series resistor is 510 Ω, which leads to a 98 mA maximum current.

- R_{5V_IMAX} = 510 Ω.
- $I_{5V,CC}$ = 98 mA.

I²C configuration

I²C is used to configure the AEM13920:

- VDDIO is connected to LOAD, which is the node supplying the application circuit that communicates with the AEM13920 through I²C.
- SDA and SCL are pulled-up to VDDIO with 1 kΩ resistors and connected to the application circuit micro controller (MCU) I²C bus.
- IRQ and ST_STO are connected to application circuit MCU GPIOs.

The configuration is sent through the I²C bus. Please note that the configuration done through pins (SRCx_CFG[4:0], STO_CFG[2:0], LOAD_CFG[2:0], etc.) must also be written to the registers, otherwise the default register values will be applied (see Section 9.11 for further details about configuring the AEM13920 with I²C registers).

See Table 64 for the whole I²C register configuration (all other registers have appropriate default values).

Temperature monitoring

Temperature monitoring is used to protect the storage element from being charged and discharged outside its acceptable temperature range. The following settings are applied:

- R_{TH}:
  - R0 = 10 kΩ.
  - BETA = 3380.
- R_{DIV} = 22 kΩ.
- Charging is allowed between 0°C and +45°C (see Table 64 for the values to write the registers).
- Discharging is allowed between -20°C and +65°C (see Table 64).
- Temperature monitoring is enabled by default (see Section 9.11.8) so it is not mandatory to write the TMON register.

Average Power Monitoring (APM)

To set up the APM, user must do the following:

- Enable the APM event in register IRQEN1 so that a rising edge is generated on the IRQ pin so that the application MCU is notified when a new APM data is ready. This is done by setting the IRQEN1.APMDONE field to 1.
- Configure the APM register:
  - APM.WINDOW = 0: computation window of 128 ms for longest integration.
  - APM.MODE = 1: power meter mode.
  - APM.BUCKEN = 1: enable power monitoring of energy from STO to LOAD.
  - APM.SRC1EN = 1: enable power monitoring of energy from SRC1 to STO.
  - APM.SRC2EN = 0: disable power monitoring of energy from SRC2 to STO.
- Read APM data when IRQ raises.
- Read the IRQFLG1 register to reset the IRQ pin.

Shipping mode

Shipping mode is not used.

- SHIP_MODE is connected to GND.

Register Name	Value	Notes
SRC1REGU1 SRC1REGU0	0x07 0x02	Constant voltage mode. $V_{SRCx,REG}$ = 0.6 V.
VOVDIS	0x15	V_{OVDIS} = 2.80 V.
VCHRDY	0x22	V_{CHRDY} = 3.10 V.
VOVCH	0x32	V_{OVCH} = 3.63 V.
BUCKCFG	0x0F	V_{LOAD} = 2.5 V. T_{MULT} = 2x.
	0x8F	Min. 0°C for charge.
		Max. +45°C for charge.
		Min. -20°C for discharge.
		Max. +65°C for discharge.
TMON	0x01	Enable temperature monitoring.
IRQEN1	0x40	Enable APMDONE IRQ.
APM	0x0D	Configure APM.
CTRL	0x01	Write this register after writing the others to load I²C register configuration.

Table 64: Summary of I²C register configuration for typical application circuit 3.

11. Circuit Behavior

11.1. Start Up from SRCx

11.1.1. Configuration:

- SRC1 supplied by a 2.0 V voltage source with 100 mA compliance with 700 Ω in series:
  - V_{OVCH} = 2.0 V.
  - V_{MPP} = 1.5 V with R_{MPPT} = 75%.
  - I_{SRC1} = 714 µA.
- SRC1_MODE = H:
  - SRC1 mode is MPPT.
- SRC1_CFG[4:3] = LH:
  - $T_{MPPT,PERIOD}$ = 512 ms.
  - $T_{MPPT,SAMPLING}$ = 8 ms.
- SRC1_CFG[2:0] = HLL:
  - R_{MPPT} = 75%.
- L_{BOOST1} = 33 µH.
- STO_CFG[2:0] = LHL:
  - V_{OVDIS} = 3.00 V.
  - V_{CHRDY} = 3.30 V.
  - V_{OVCH} = 4.12 V
- C_{STO} = 1 mF electrolytic charged at 2.8 V beforehand.
- LOAD_CFG[2:0] = HLH:
  - V_{LOAD} = 1.8 V.
- L_{BUCK} = 10 µH.
- VDDIO = 3.3 V (external source).

11.1.2. Observations

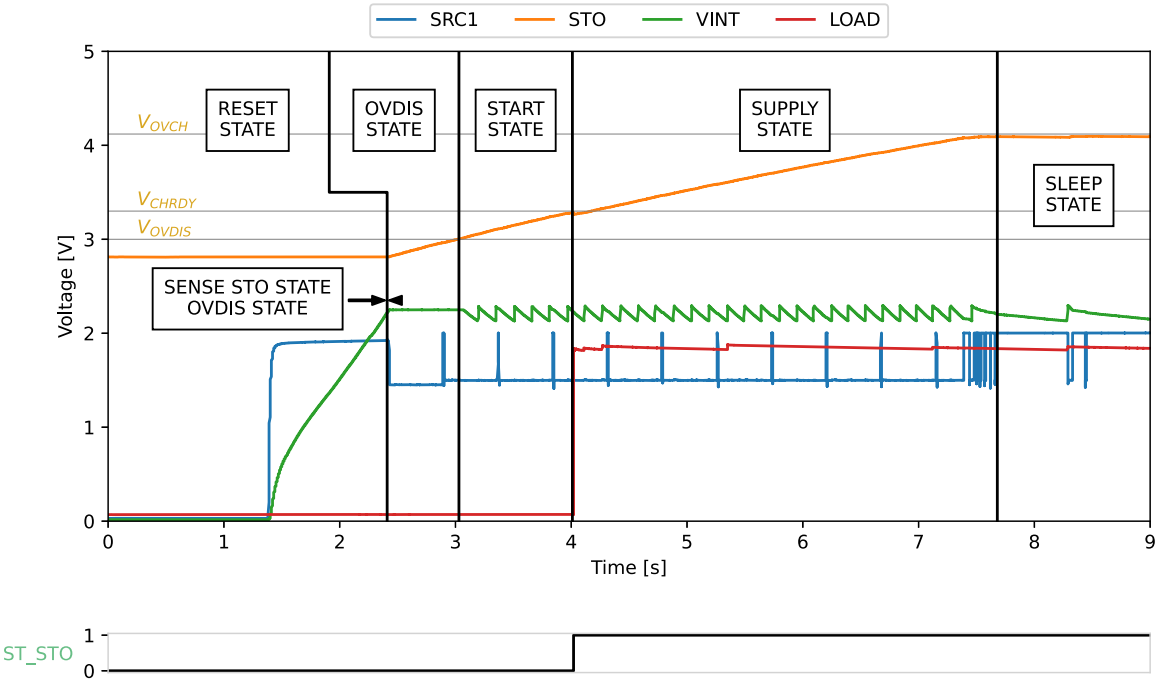


Figure 15: AEM13920 behavior at start up

- The AEM13920 is initially in RESET STATE.
- Once the supply connected on SRC1 is switched on, the AEM13920 coldstarts. C_{INT} is charged until VINT reaches $V_{INT,CS}$. The AEM13920 switches then to SENSE STO STATE.
- In SENSE STO STATE, the AEM13920 measures V_{STO}, which is slightly below V_{OVDIS}. The AEM13920 switches then to OVDIS STATE.
- In OVDIS STATE, the AEM13920 performs a first V_{OC} evaluation and charges the storage element on STO by harvesting the energy from SRC1. V_{SRC1} is regulated at 75% of V_{OC}, thanks to the MPPT module. VINT is supplied by SRC1. Once V_{STO} reaches V_{OVDIS}, the AEM13920 switches to START STATE.
- In START STATE, the AEM13920 charges the storage element connected to STO. The MPPT module still ensures that V_{SRC1} is regulated at 75% of V_{OC}. The LOAD output is disabled. VINT is supplied by STO. Once V_{STO} reaches V_{CHRDY}, the AEM13920 switches to SUPPLY STATE.
- In SUPPLY STATE, the AEM13920 behaves as in START STATE and keeps charging the storage element. The LOAD output is enabled, so that V_{LOAD} is regulated at 1.8 V. Once V_{STO} reaches V_{OVCH}, the AEM13920 switches to SLEEP STATE.
- In SLEEP STATE, STO, LOAD and VINT are fully charged. The AEM13920 stops harvesting energy from SRC1. Please note that around 8.3 s, the AEM13920 recharges VINT from SRC1, and around 5.5 s, the AEM13920 switches briefly to SUPPLY STATE to recharge STO from SRC1.

11.2. Shutdown

11.2.1. Configuration:

- SRC1 supplied by a 2.0 V voltage source with 100 mA compliance with 500 Ω in series:
  - V_{OVCH} = 2.0 V.
  - V_{MPP} = 1.5 V with R_{MPPT} = 75%.
  - I_{SRC1} = 1 mA.
  - The supply is disconnected near 13 s.
- SRC1_MODE = H:
  - SRC1 mode is MPPT.
- SRC1_CFG[4:3] = LH:
  - $T_{MPPT,PERIOD}$ = 512 ms.
  - $T_{MPPT,SAMPLING}$ = 8 ms.
- SRC1_CFG[2:0] = HLL:
  - R_{MPPT} = 75%.
- L_{BOOST1} = 33 µH.
- STO_CFG[2:0] = LHL:
  - V_{OVDIS} = 3.00 V.
  - V_{CHRDY} = 3.30 V.
  - V_{OVCH} = 4.12 V
- C_{STO} = 10 mF electrolytic capacitor charged at 2.8 V beforehand.
- LOAD_CFG[2:0] = HLH:
  - V_{LOAD} = 1.8 V.
  - A 200 Ω resistor is connected between LOAD and GND, so that a 9 mA current is pulled from the LOAD pin (negative .
- L_{BUCK} = 10 µH.
- VDDIO = 3.3 V (external source).

11.2.2. Observations

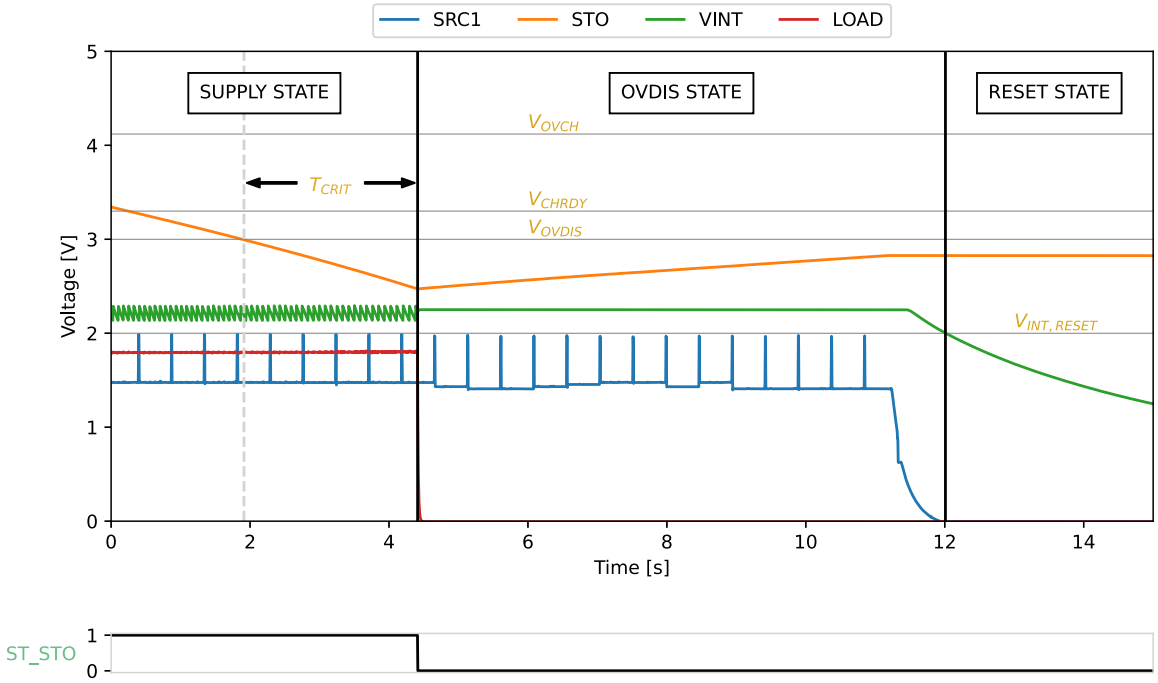


Figure 16: AEM13920 behavior at shutdown

- The AEM13920 is initially in SUPPLY STATE. ST_STO is HIGH in that state. The harvested power on SRC1 is lower than the power supplied by LOAD, so that the storage element on STO is being discharged. Once V_{STO} drops below V_{OVDIS}, the AEM13920 stays in SUPPLY STATE for T_{CRIT} and then switches to OVDIS STATE.
- In OVDIS STATE, the LOAD output is disabled and VINT is supplied by SRC1. ST_STO is LOW in that state. There is no more current drawn on the LOAD pin, and thus on the storage element on STO, so that the power budget is positive and the storage element is charged.
- Near 11.2 s, the power supply connected on SRC1 is switched off. The storage element on STO is no longer charged, neither is VINT. When V_{INT} drops below $V_{INT,RESET}$, the AEM13920 switches to RESET STATE.
- In RESET STATE, the energy present on the storage element is preserved as the STO pin is set to high impedance.

11.3. Start Up from 5V_IN

11.3.1. Configuration:

- 5V_IN supplied by a 5.0 V voltage source with 1 A compliance. A 370 Ω resistor is installed between 5V_IMAX and GND so that the current to charge the storage element on STO is limited to 135 mA.
- SRCx are left floating.
- STO_CFG[2:0] = LHL:
  - V_{OVDIS} = 3.00 V.
  - V_{CHRDY} = 3.30 V.
  - V_{OVCH} = 4.12 V.
- C_{STO} = 5 F supercapacitor charged at 2.8 V beforehand.
- LOAD_CFG[2:0] = HLH:
  - V_{LOAD} = 1.8 V.
- L_{BUCK} = 10 µH.
- VDDIO = 3.3 V (external source).

11.3.2. Observations

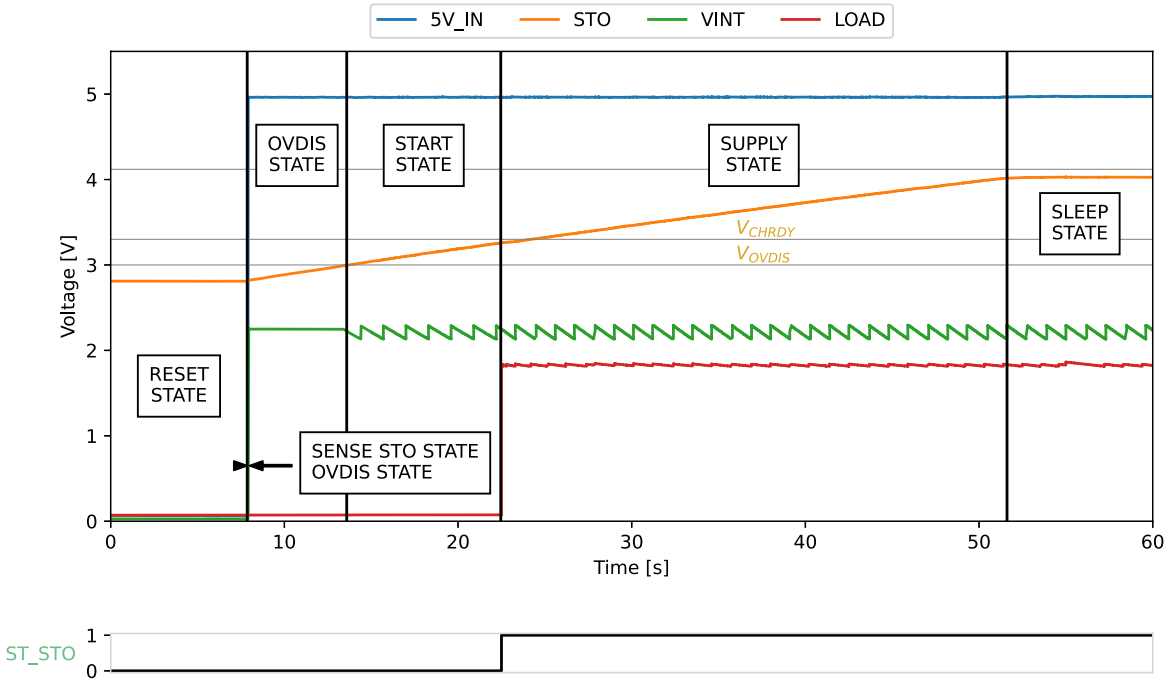


Figure 17: behavior at start up

Observations are the same as for start up from SRCx described in Section 11.1.2.

- Cold start is very fast as high power is available from 5V_IN: V_{INT} rises from 0 V to 2.2 V in about 5 ms.
- The 5 F supercapacitor is charged from below V_{OVDIS} to V_{OVCH} in about 45 s. The 5 V charger circuit stops charging the storage element about 100 mV below V_{OVCH} for safety reasons.

12. Performance Data

12.1. Boost Converter Conversion Efficiency

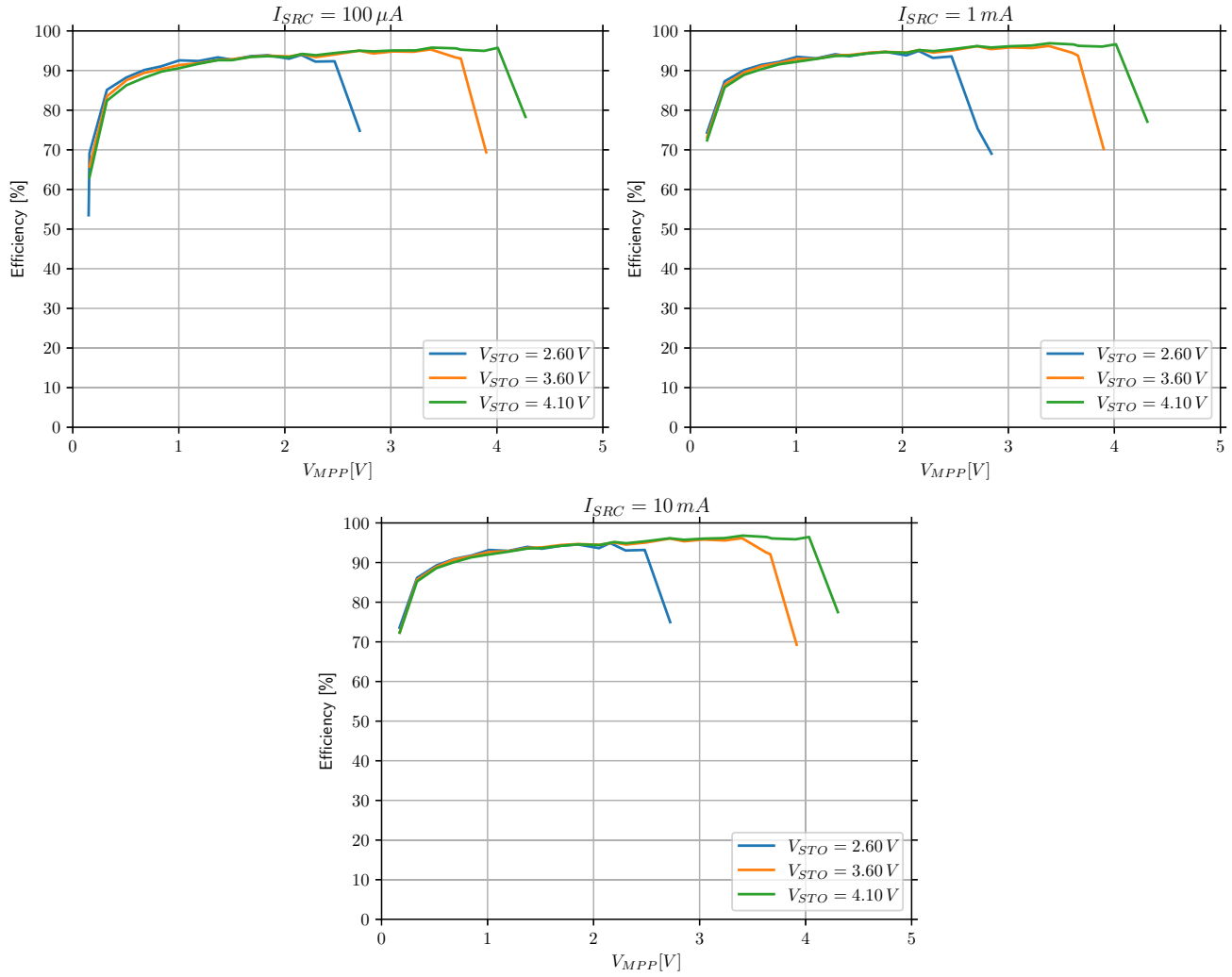


Figure 18: Boost converter efficiency with L_{BOOSTx} = 33 µH (Coilcraft LPS4018-333MRB), BSTxCFG.TMULT = 0x02 (x3)

12.2. Buck Converter Conversion Efficiency

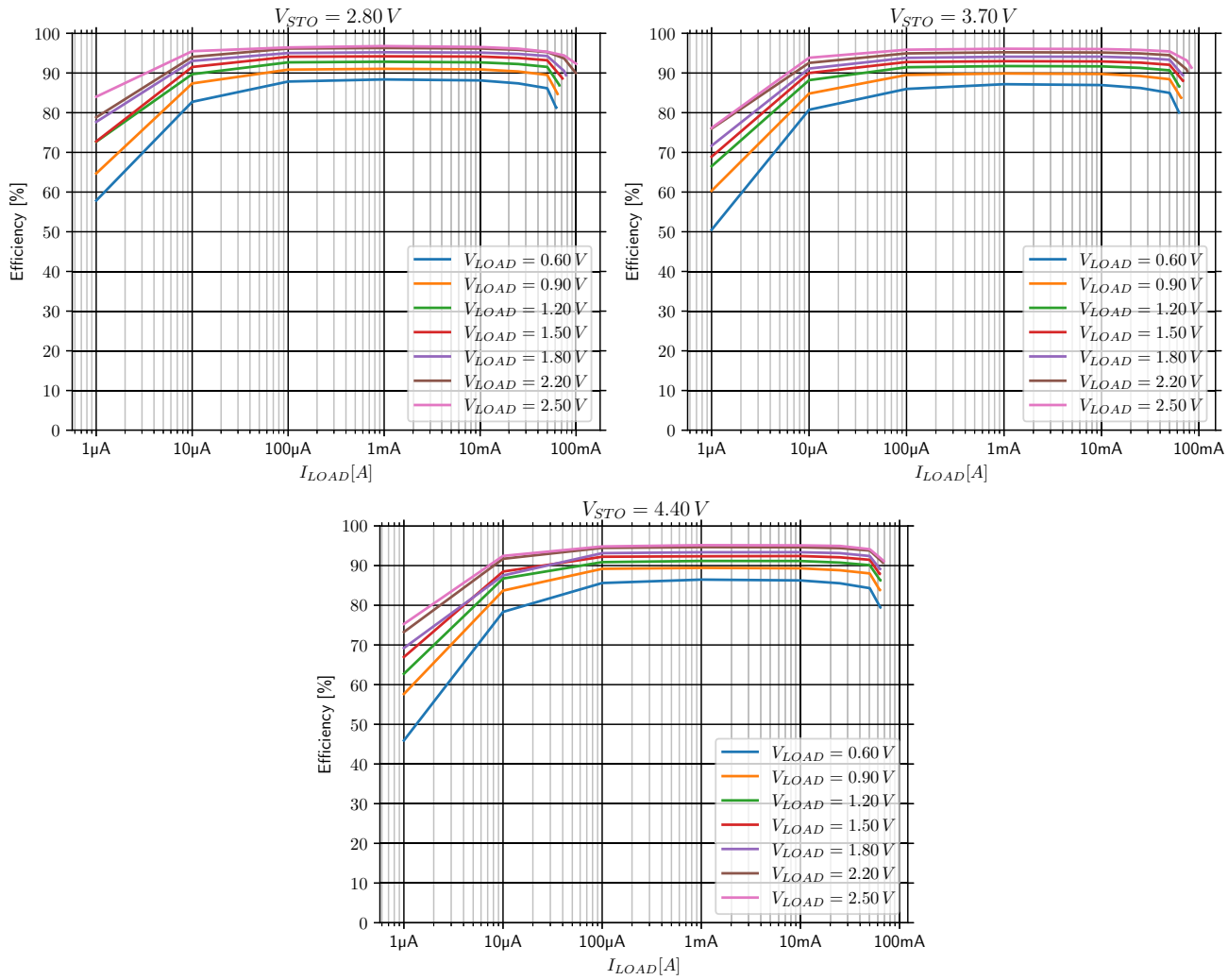


Figure 19: Buck (LOAD) converter efficiency with L_{BUCK} = 10 µH (Coilcraft LPS4018-103MRB), BUCKCFG.TMULT = 0x01 (x2)

Figure 19 efficiency is shown with the AEM13920 boost-related quiescent current subtracted from the current provided on STO:

- This quiescent current is measured with the boost converter in SLEEP STATE and with the buck converter switched off, so that the current that is necessary to run the buck converter is considered in Figure 19 data.
- It is considered in the boost efficiency data shown in Section 12.1.

13. Minimum BOM

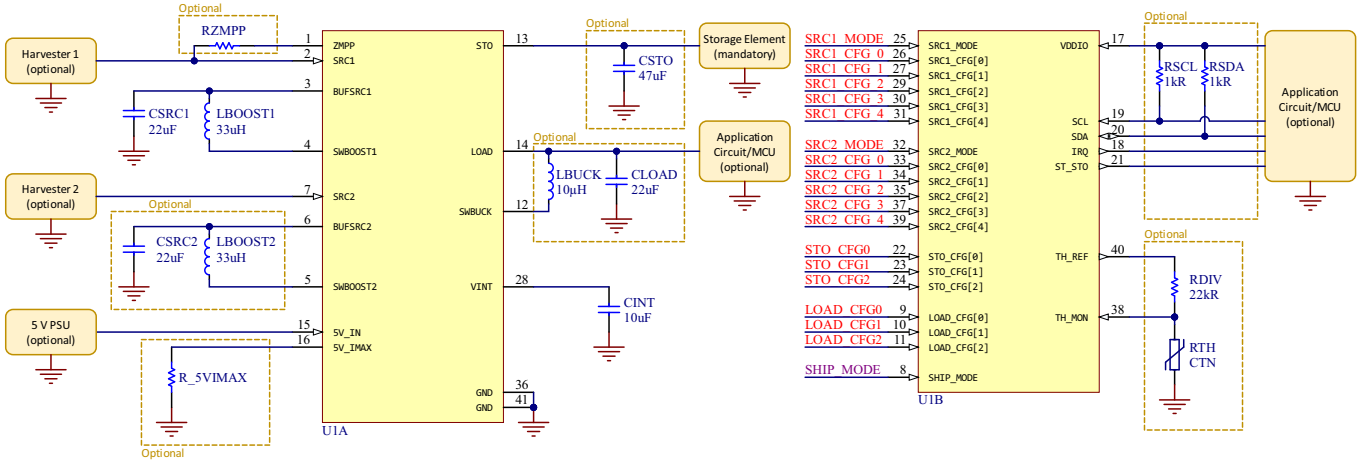


Figure 20: AEM13920 schematic

Designator		Description	Quantity	Manufacturer	Part Number
Mandatory	U1	AEM13920	1	e-peas	order at sales@e-peas.com
	Storage Element	Min. voltage 2.4 V Max. voltage 5.0 V	1	To be defined by user.	
	CINT	Ceramic capacitor 10 µF, 6.3 V, 20%, X5R, 0402	1	Murata	GRM155R60J106ME44D
	CSRC1	Ceramic capacitor 22 µF, 10 V, 20%, X5R, 0603	1	Murata	GRM188R61A226ME15D
	LBOOST1	Power Inductor 33 µH - 0.68 A	1	Coilcraft	LPS4018-333MRB
Optional	RZMPP[1]	Resistor	1	To be defined by user.	
	CSRC2[1]	Ceramic capacitor 22 µF, 10 V, 20%, X5R, 0603	1	Murata	GRM188R61A226ME15D
	LBOOST2[1]	Power inductor 33 µH - 0.68 A	1	Coilcraft	LPS4018-333MRB
	R_5VIMAX[1]	Resistor	1	To be defined by user.	
	CSTO[2]	Ceramic capacitor 47 µF 6.3 V 20% X5R, 0603	1	Murata	GRM188R60J476ME15D
	CLOAD	Ceramic capacitor 22 µF, 10 V, 20%, X5R, 0603	1	Murata	GRM188R61A226ME15D
	LBUCK	Power inductor 10 µF	1	TDK	VLS252012CX-100M-1
	RSCL	Resistor 1 kΩ	1	Multicomp	MCWR06X1001FTL
	RSDA	Resistor 1 kΩ	1	Multicomp	MCWR06X1001FTL
	RDIV	Resistor 22 kΩ	1	Yageo	PNRC0402FR-0722KL
	RTH	10 kΩ NTC thermistor	1	Murata	NCP15XH103J03RC

Table 65: Minimum BOM

1. The AEM13920 must have at least one energy source to work: boost #1 (SRC1), boost #2 (SRC2) or 5 V input (5V_IN), or any combination of those.
2. CSTO is not mandatory but ensures high boost converter efficiency with high ESR storage elements.

14. Package Information

14.1. Package Dimensions

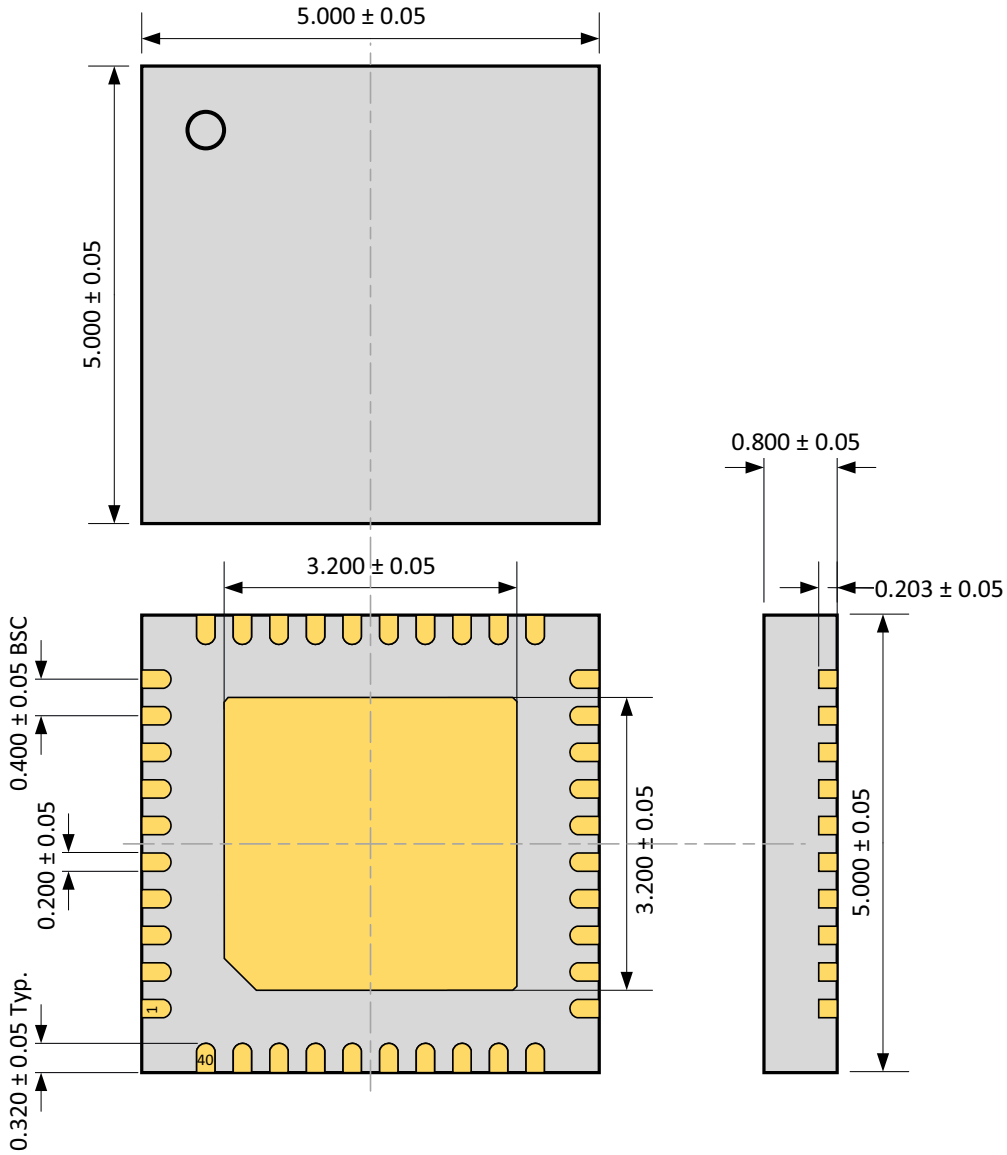


Figure 21: QFN 40-pin 5x5mm drawing (all dimensions in mm)

15. Glossary

15.1. SRCx Acronyms

V_{SRCx}

Voltage on the SRCx pin.

$V_{SRCx,CS}$

Minimum voltage required on SRCx for the AEM13920 to coldstart.

$V_{SRCx,REG}$

Target regulation voltage of the source, depending on SRCx_CFG[4:0] configuration or I²C register (when SRCx regulation mode is constant voltage).

V_{MPP}

Target regulation voltage on SRCx when extracting power (when SRCx regulation mode is MPPT).

V_{OC}

Open circuit voltage of the harvester connected on SRCx.

$V_{SLEEP,THRESH}$

Sleep threshold voltage as described in Section 9.11.9.

C_{SRCx}

Decoupling capacitor on BUFSRCx pin.

I_{SRCx}

Current extracted from the harvester connected on SRCx.

L_{BOOSTx}

Boost converter x inductor.

R_{MPPT}

For the boost converters, ratio between the open circuit voltage V_{OC} and the voltage regulation V_{MPP} determined by the MPPT (when the boost converter is in MPPT mode).

$I_{LBOOST,PEAK}$

Peak current in L_{BOOSTx} when the boost converter is running.

$T_{MPPT,PERIOD}$

Time between two MPP evaluations (see Table 10).

$T_{MPPT,SAMPLING}$

Open-circuit duration for the MPP evaluations (see Table 10).

R_{ZMPP}

Resistor used for ZMPP module, connected between SRC1 and ZMPP.

15.2. STO Acronyms

V_{STO}

Voltage on the STO pin.

V_{OVDIS}

Minimum voltage accepted on the storage element before stopping to supply LOAD (see Section 9.4).

V_{CHRDY}

Minimum voltage accepted on the storage element before starting to supply LOAD in START STATE (see Section 9.4).

V_{OVCH}

Maximum voltage accepted on the storage element before disabling its charging (see Section 9.4).

C_{STO}

Decoupling capacitor on STO pin.

I_{QSHIP}

Quiescent current drawn on the storage element when the AEM13920 is in shipping mode (SHIP_MODE is HIGH).

$I_{QSHIP,SRCx}$

Current drawn on the storage element when the AEM13920 is in shipping mode and energy is available on SRCx.

15.3. VINT Acronyms

V_{INT}

Voltage on the VINT pin.

$V_{INT,CS}$

Minimum voltage on VINT to allow the AEM13920 to switch from RESET STATE to SENSE STO STATE.

$V_{INT,RESET}$

Minimum voltage on VINT before switching to RESET STATE (from any other state).

C_{INT}

Decoupling capacitor on VINT pin.

I_{QSLEEP}

Quiescent current drawn on STO when the AEM13920 is in SLEEP STATE.

$I_{QSUPPLY}$

Quiescent current drawn on STO when the AEM13920 is in SUPPLY STATE.

15.4. I²C Acronyms

V_{VDDIO}

Voltage on the VDDIO pin.

15.5. LOAD Acronyms

V_{LOAD}

Voltage on the LOAD pin.

C_{LOAD}

Decoupling capacitor on LOAD pin.

L_{BUCK}

Buck converter inductor.

$I_{LBUCK,PEAK}$

Peak current in L_{BUCK} when the buck converter is running.

15.6. 5V_IN Acronyms

V_{5V_IN}

Voltage on 5V_IN pin.

$V_{5V\_IN,MIN}$

Minimum voltage on 5V_IN pin.

$I_{5V,CC}$

Current provided to the storage element by the 5V_IN when in constant current mode.

$I_{5V,CV}$

Current provided to the storage element by the 5V_IN when in constant voltage mode.

R_{5V_IMAX}

Resistor connected between 5V_IMAX and GND that defines the maximum current provided to the storage element by the 5 V charger (5V_IN pin).

15.7. Various Acronyms

E_{APM}

Energy measured by the APM module.

R_{TH}

Along with R_{DIV}, thermistor creating a resistive voltage divider connected to TH_MON, used for thermal monitoring.

R_{DIV}

Along with R_{TH}, resistor creating a resistive voltage divider connected to TH_MON, used for thermal monitoring.

R_{SCL} / R_{SDA}

Pull-up resistors used for the I²C communication bus.

T_A / T_B

Respectively, duration of APM phase A and B.

T_{CRIT}

In SUPPLY STATE, the AEM13920 waits for T_{CRIT} before switching to OVDIS STATE when V_{STO} drops below V_{OVDIS}.

$T_{GPIO,MON}$

GPIO reading rate.

T_{MULT}

Boost or buck converter inductor charging timng multiplier.

$T_{TEMP,MON}$

Temperature monitoring rate.

16. Revision History

Revision	Date	Description
1.0	April, 2023	Creation of the document.
1.1	August, 2023	Finished register descriptions. Added: - I²C protocol. - Efficiencies. - Behavior graphs. - Typical application circuits. - Glossary. - Quiescent currents.
1.2	September, 2023	Added: - Missing storage element voltage info on buck efficiency graph. - Boost efficiency graph: source current as graph title instead of x axis title. - Minimum BOM section. - Updated minimum cold-start power.

Table 66: Revision History