

## AU6122: 800 mW Driver Amplifier, 2.3 – 4.2 GHz

### General Description

The AU6122 is a wideband 800mW driver amplifier suitable for application in FDD and TDD wireless infrastructure and general-purpose amplification over a wide frequency range of 1.8 to 5.0GHz. The RF input and output ports are internally matched to 50Ω for the full frequency range. This device incorporates a device enable pin with turn on/off times less than 1 $\mu$ s.

The driver amplifier has high gain and linearity and will support a high instantaneous bandwidths required for 5G NR carrier aggregated signals. The device linearizes well in DPD systems. Linearized on its own it will provide better than 50 dBc ACLR for a 20MHz 5G NR.

### Applications

- 4G/5G infrastructure applications multiple 3GPP bands
- MIMO Systems
- General purpose amplification

### Features

- Extremely Wideband – 2.3 to 4.2 GHz
- High Peak Power – 29 dBm
- Low Bias Current – 110 mA
- High Small Signal Gain – 37 dB
- Supports Carrier Aggregation for 4G/5G
- Shutdown / Enable Pin
- Single Supply +5.0 V, adjustable I<sub>cc</sub>
- Package: 3x3 mm

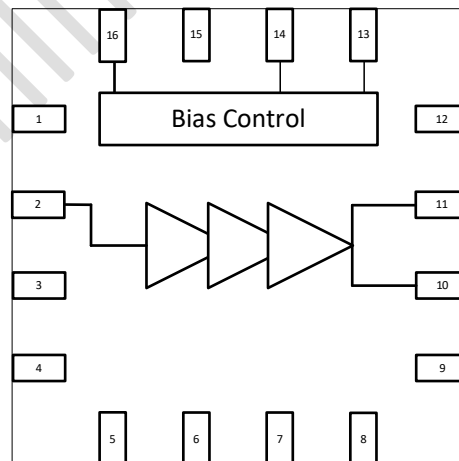


Figure 1 Functional Diagram

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## 1 Pin Configuration

### 1.1 Pin Configuration Diagram

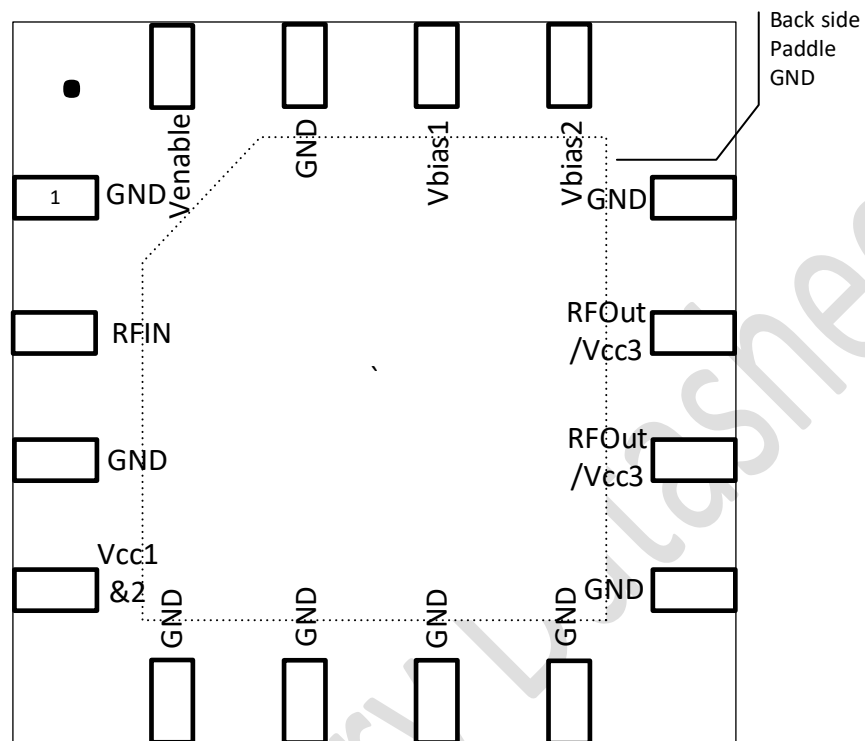


Figure 2 AU6122 Pin Diagram (top view)

## 1.2 Pin Description

**Table 1 Pin Description**

Pin Name	Pin No	I/O Type	Description
GND	1		Internally connected to Ground
RFIN	2		RF Input – Matched to 50Ω
GND	3		Internally connected to Ground
Vcc1 & 2	4		Collector connection to stages 1 & 2
GND	5		Internally connected to Ground
GND	6		Internally connected to Ground
GND	7		Internally connected to Ground
GND	8		Internally connected to Ground
GND	9		Internally connected to Ground
RF Out/Vcc3	10		RF Output – Matched to 50Ω, Collector connection to stage 3
RF Out/Vcc3	11		Internally connected to Pin 10
GND	12		Internally connected to Ground
Vbias1	13		Supply for bias circuit
Vbias2	14		Control input to adjust quiescent bias current – see
GND	15		Internally connected to Ground
Venable	16		Toggles between ON state and low power state Hi=Device On, Low=Device Off
Backside Paddle-	GND		This is the ground connection and should be soldered directly to ground

## 2 Electrical Specifications

**Table 2 Absolute Maximum Ratings**

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage				5.5	V
Control Pin Input Voltage				2.5	V
Peak RF Input Power (RFIN)				10	dBm
Maximum Junction Temperature				150	°C
Storage Temperature		-55		125	°C
ESD voltage HBM, all pins				1000	V

**Notes:**

- Exceeding absolute maximum ratings listed in Table 1 may cause permanent damage.
- Operation should only occur within the limits specified in Table 2. Operating between the maximum operating range and the absolute maximum for extended periods may reduce the reliability of the product.
- Observe standard procedures as with other ESD-sensitive devices when handling the product. The product includes ESD protection circuitry, but precautions should be taken not to exceed the ratings specified in above table.

**Table 3 Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage (VCC1,2,3, Vbias1,2)		4.75	5	5.25	V
Quiescent Current (ICC), see notes			130		mA
Control Input High		1.5	1.8		V
Control Input Low		0		0.7	V
Control Input Currents			1	12	μA
RF Input Power, average				-20	dBm
RF Input Power, peak				-11.5	dBm
Operating Temperature Range (Tcase)		-40	25	105	°C

**Notes:**

- This table lists the recommended conditions. The product should not be operated outside these recommended operating conditions.
- Quiescent current is programmable, see Table 6.

**Table 4 Electrical Characteristics**

This table provides key electrical specifications at Tcase=25°C, VCC = VBIAS = 5V, Icc=130mA unless otherwise specified.

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Frequency		f	2300		4200	MHz
Small Signal Gain	P <sub>IN</sub> = -35 dBm, 2300 MHz	S21		37		dB
	P <sub>IN</sub> = -35 dBm, 2600 MHz			37		
	P <sub>IN</sub> = -35 dBm, 3600 MHz			37		
	P <sub>IN</sub> = -35 dBm, 4200 MHz			37		
Input Return Loss	P <sub>IN</sub> = -35 dBm	S11		12		dB
Output Return Loss	P <sub>IN</sub> = -35 dBm	S22		10		dB
Reverse Isolation	P <sub>IN</sub> = -35 dBm	S12		50		dB
Gain Flatness	In any 100 MHz bandwidth, P <sub>in</sub> = -35 dBm	Gflat		0.5		dB
ACLR (without DPD)	5G NR 20 MHz, 8.5 dB PAR, +15.0 dBm av. Power, F = 2600 MHz	ACLR		-40		dBc
ACLR (without DPD)	5G NR 20 MHz, 8.5 dB PAR, +15.0 dBm av. Power, F = 3600 MHz	ACLR		-40		dBc
Output Power at 1dB compression. Pulsed using 10us/100us (on/off duty cycle)	At 2.3 GHz	P1dB		25		dBm
	At 2.6 GHz			26		
	At 3.6 GHz			26		
	At 4.2 GHz			26		
Output Power at 3dB compression. Pulsed using 10us/100us (on/off duty cycle)	At 2.3 GHz	P3dB		26		dBm
	At 2.6 GHz			27		
	At 3.6 GHz			29		
	At 4.2 GHz			29		
Noise Figure	At 3.6 GHz	NF		6		dB
Off current	Venable = 0 V	ICCQ_OFF		4		mA
Turn-on time	50% Venable to 90% RF Power	Ton			1	us

### 3 Schematic Diagram

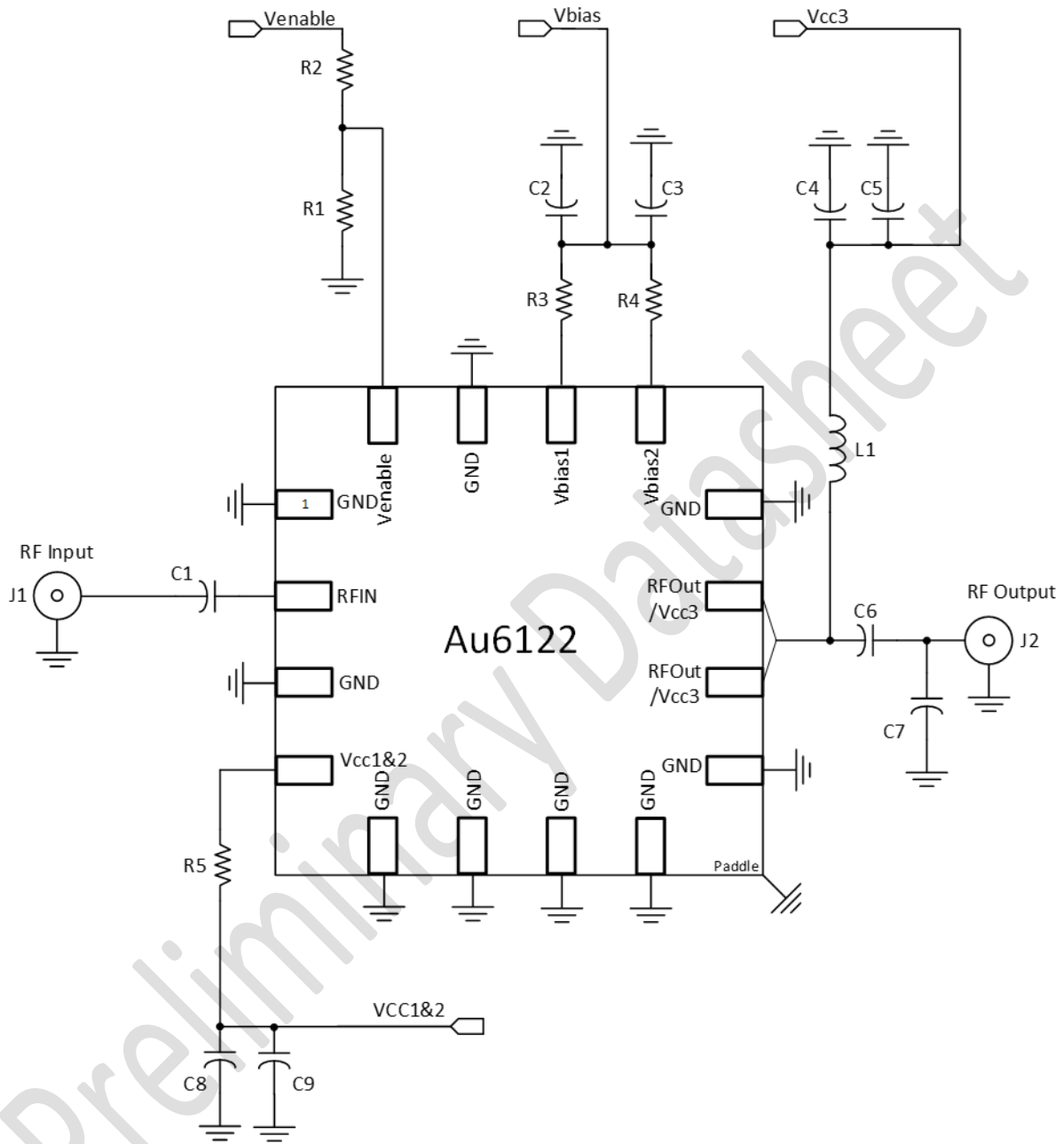


Figure 3 Schematic Diagram

**Table 5 Bill of Materials**

Reference Designator	Value	Description	Part Number	Mfr
C1, C6	18pF	50V 5% 0402	GRM1555C1H180JB01	MuRata
C5, C9	1uF	16V 10% X6S 0402	GRM155C81C105KE15	MuRata
C2, C3, C4, C8	100pF	50V 5% 0402	GRM1555C1H101JB01	MuRata
C7	DNF			
R1	DNF			
R3	1k8	62mW 0402		Various
R2, R4, R5	0 Ohm	100mW 0402		Various
L1	12nH	5% 640mA	0402DC-12NXJLW	Coilcraft
J1, J2	SMA	Female End Launch	142-00701-851	

**Table 6 Iccq vs R3 Value**

R3			1k8		
Icc (mA)			130		



## 4 Package Information

Package Dimensions shown below.

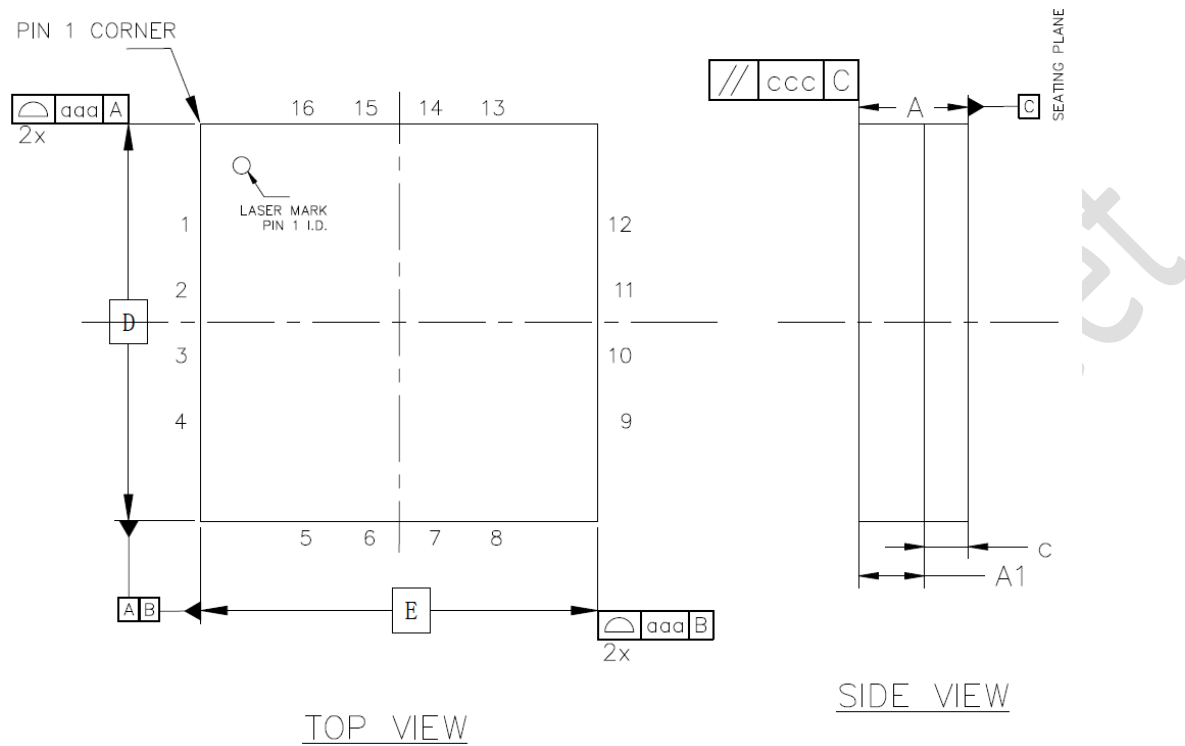


Figure 4 - Package Drawing

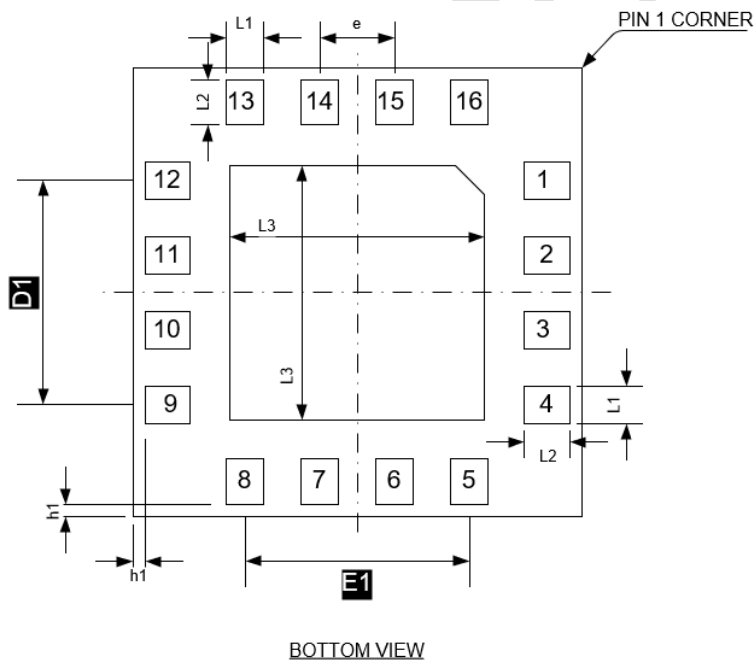


Figure 5 - Pin Details

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.767	0.827	0.887
A1	0.50BASIC		
c	0.297	0.327	0.357
E	2.900	3.000	3.100
D	2.900	3.000	3.100
E1	1.50 BASIC		
D1	1.50 BASIC		
e	0.50 BASIC		
L1	0.200	0.250	0.300
L2	0.250	0.300	0.350
L3	1.650	1.700	1.750
h1	0.08 REF		
aaa	0.150		
ccc	0.080		

## 5 Recommended PCB Footprint

The paste stencil has the same pad sizes as the component package detailed above.

Solder Mask Pads are 50um larger per edge.  
 For example 300um x 250um pads are increased to 400um x 350um.  
 Ground Paddle is defined as L3 (1.7mm)

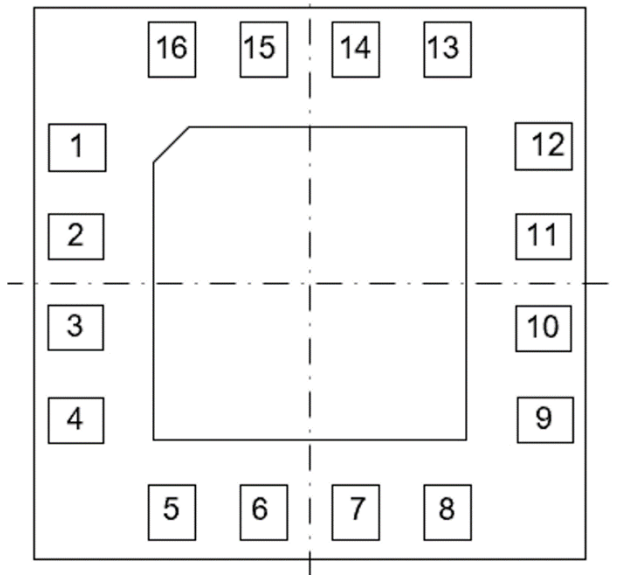


Figure 6 - Stencil Aperture Top View

Component footprint uses same size pads as package outline

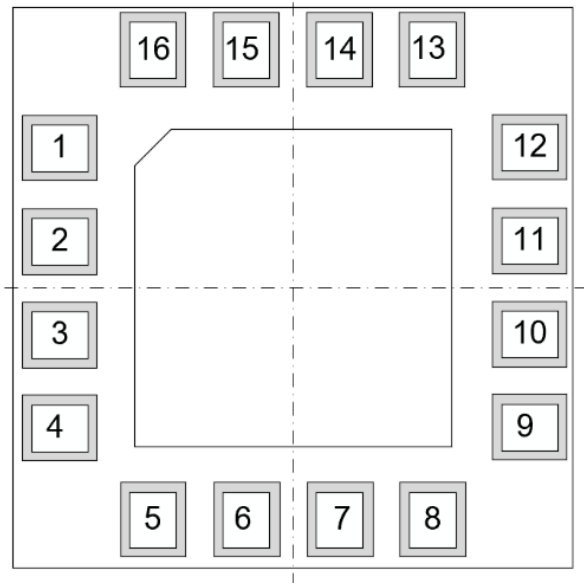


Figure 8 - Solder Mask Top View

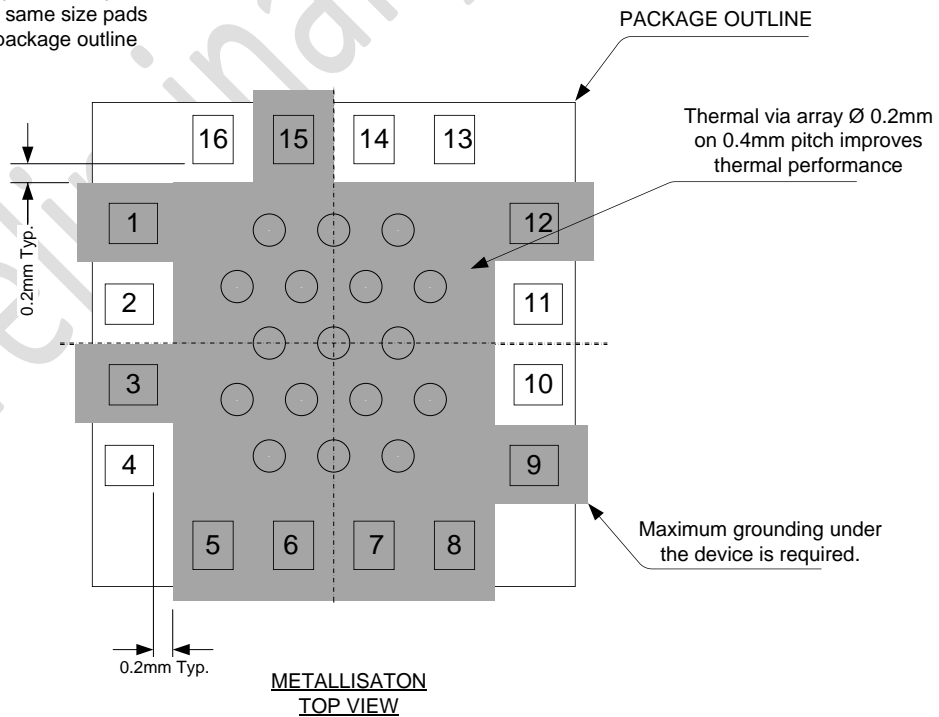


Figure 7 - Metalisation Top View

## 6 Tape and Reel Information

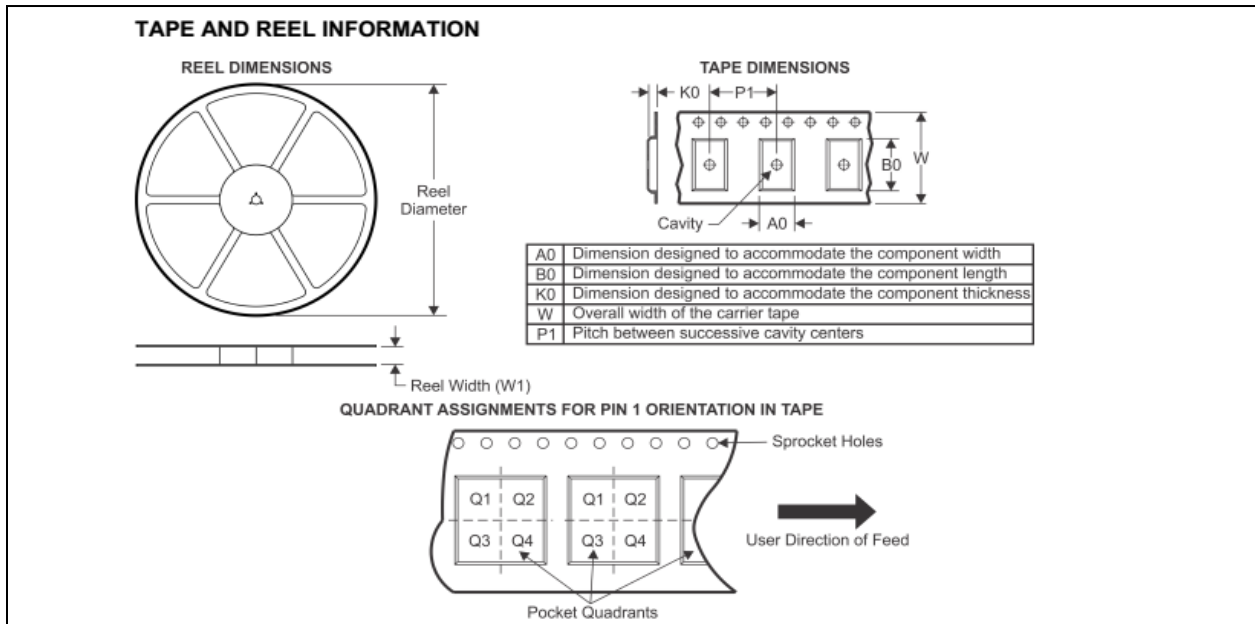


Figure 9 Carrier and Cover Tape Dimensions

Table 7 Carrier and Cover Tape Dimensions

Package type	Pins	Pin1 Quadrant	SPQ	Reel Diameter	Reel Width	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
LGA3x3	16	Q1	TBD	178	12.4	3.3	3.3	1.1	4	12

## 7 Ordering Information

Table 8 Ordering Information

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temperature Range
AU6122-LMR	AU6122		Tape and Reel	

## 8 Revision History

Table 9 Revision History

Version Number	Date	Description	Author
8		AU6122 Datasheet Created	Aurasemi

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