AU1311

Datasheet

Features:

- Full-scale up to ±16g
- Measurement range configurable
- TDM/SPI/I2C interfaces
- Signal bandwidth 3000Hz (TDM)
- Low-noise
- 16-bit data output

Application:

- Bone vibration detection
- Beam forming enhancement
- Voice detection enhancement

Description:

The AU1311 is a low-noise, high-bandwidth, 3-axis digital accelerometer with full scale measurement at up to ±16g.

The digital output data of the sensor is formatted as 16-bit two's complement and is accessible through TDM/SPI/I2C interface.

External host can configure the sensor by SPI/I2C interface.

The AU1311 is well suited for hearables like smart earbuds.

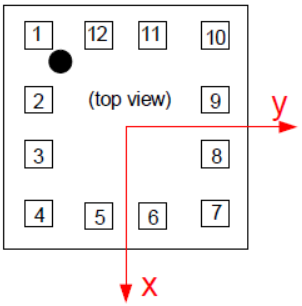
The device is in 2×2×0.86mm LGA package with 12 pins. It can operate in temperature range from -40℃ to 85℃.

Contents

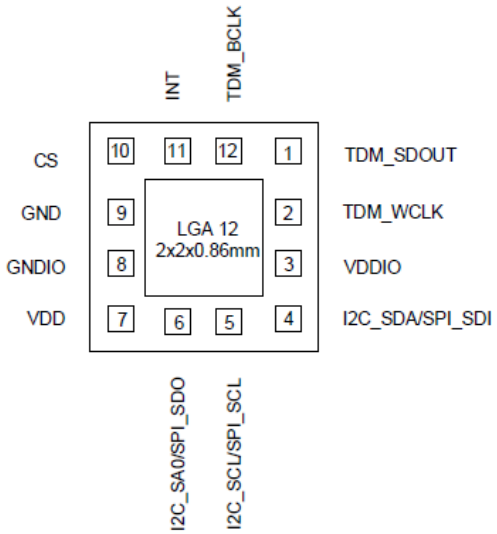
1. PIN description

Pin Number	Type	Pin Name	Function
1	O	TDM_SDOUT	TDM serial data output
2	I	TDM_WCLK	TDM word clock
3	I	VDDIO	Digital IO supply voltage
4	IO	I2C_SDA/SPI_SDI	I2C Data (SDA), SPI serial data input
5	IO	I2C_SCL/SPI_SCL	I2C and SPI serial clock (SCL)
6	IO	I2C_SA0/SPI_SDO	I2C slave address, SPI serial data output
7	I	VDD	Power supply
8	I	GNDIO	Ground for IO
9	I	GDN	Ground for supply
10	I	CS	I2C and SPI selection (testPin1)
11	O	INT	Interrupt (testPin2)
12	I	TDM_BCLK	TDM bit clock

Top view:



Bottom view:



2. Mechanical and electrical specifications

2.1 Mechanical characteristics

Parameter	Notes	Min	Typ	Max	Unit
Full scale input (FS)	FS=00		±2		g
	FS=01		±4		
	FS=10		±8		
	FS=11		±16		
Sensitivity (Scale Factor)	FS=00, 16-bit output		61		µg/LSB
	FS=01, 16-bit output		122		
	FS=10, 16-bit output		244		
	FS=11, 16-bit output		488		
Temperature coefficient of offset (TCO)	over temperature -40℃ to 85℃, at board level	-3.5		+3.5	mg/℃
Temperature coefficient of sensitivity (TCS)		-0.08		+0.08	%/℃
Initial offset tolerance	board level	-300		+300	mg
Noise density	BW=3kHz		25		µg/rtHz
RMS noise	BW=3kHz			1.4	mg_rms
Non-linearity	best fit line	-2		+2	%
THD and noise	with 1kHz sinusoidal 1g peak input			1	%
System bandwidth in TDM mode	±0.5dB	3000			Hz
System bandwidth in SPI mode	±3dB		0.5*ODR		Hz
Mechanical resonant frequency (±3dB)	with electrical softening		4500		Hz

2.2 Electrical characteristics

Parameter	Notes	Min	Typ	Max	Unit
Supply voltage VDD		1.71	1.8	1.99	V
Supply voltage VDDIO		1.2	1.8	1.99	V
Power down current	No external clock switching		0.5		μA
Low power wake-up (sniff) mode current	For wake-up motion detection		5		μA
Normal mode power consumption	1-axis mode, z axis		600		μA
	2-axis mode, x or y and z		700		
	3-axis mode, x, y & z		800		
SPI mode ODR	With SPI interface (3bit ODR control)		31.25		Hz
			62.5		
			125		
			250		
			1000		
			2000		
			4000		
TDM mode ODR	TDM_BLK=1.024MHz		8		kHz
	TDM_BLK=2.048MHz		16		
	TDM_BLK=3.072MHz		24		
Startup time				10	ms
VIH	Digital high-level input voltage	0.7* VDDIO			V
VIL	Digital low-level input voltage			0.2* VDDIO	V
VOH	High-level output voltage	VDDIO - 0.2			V
VOL	Low-level output voltage			0.2	V
Operation temperature range		-40		+85	℃

3. TDM interface

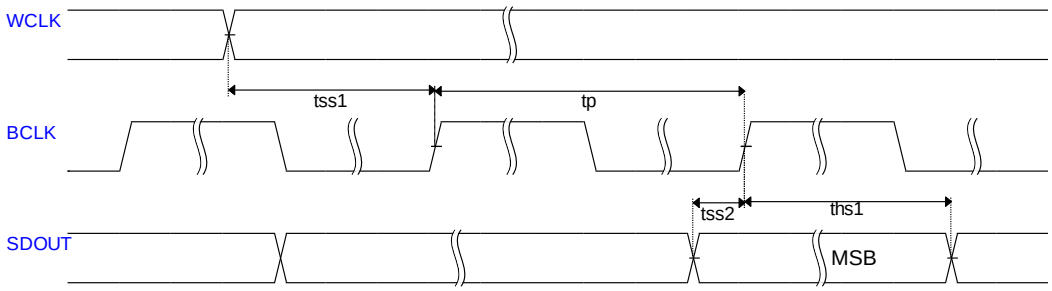
3.1 TDM protocol

The Time Division Multiplexed (TDM) interface enables transmitting multiple channels of data on a single data line between devices by separating signal data into different frames. TDM interface consists of two clock signals (WCLK and BCLK) and one data signal (SDOUT). Data frames are synchronized by WCLK, while data bits within a frame are synchronized by BCLK.

In the case of AU1311, WCLK and BCLK clocks are provided by master device, and accelerometer data are sent on SDOUT. The ratio between BCLK and WCLK is fixed to 128, namely, a data frame contains 128 bits. Since the raw data of axes are represented as 16-bit signed integers in two's complement format, a data frame can be divided into 8 slots to hold output data. The AU1311 has three slots carrying data while the other empty slots are in high impedance. The X/Y/Z axis data are allocated to SLOT0/4, SLOT1/5 and SLOT2/6 respectively depending to the mapping setting in TDM_CFG0.

3.2 TDM interface characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
BCLK	BCLK frequency ($1/t_p$)	WCLK=8kHz		1.024		MHz
		WCLK=16kHz		2.048		
		WCLK=24kHz		3.072		
WCLK8	8kHz WCLK mode			8		kHz
WCLK16	16kHz WCLK mode			16		kHz
WCLK24	24kHz WCLK mode			24		kHz
PDC	All clock pin duty cycle (except WCLK)		45		55	%
WT	WCLK setup time before BCLK rising or falling edge (tss1)		20			ns
SDOST	SDOUT setup time before BCLK rising or falling edge (tss2)		15			ns
SDOHTR	SDOUT hold time after BCLK rising or falling edge (ths1)		15			ns
SDOHTZ	SDOUT hold time of LSB after BCLK rising or falling edge (ths2)		15		50	ns
C_{BCLK}	BCLK pin capacitance				10	pF
C_{WCLK}	WCLK pin capacitance				10	
C_{SDOUT}	SDOUT load capacitance				60	
FRREL	Relative frequency response		-0.5		0.4	dB



3.2 TDM configuration

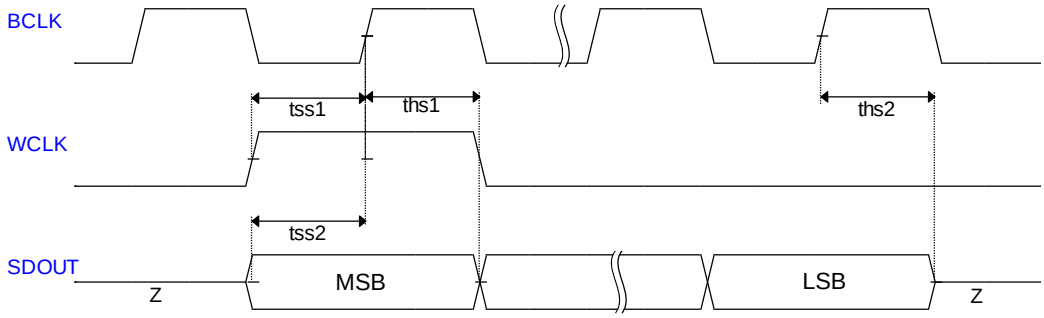
Four TDM configurations are supported by AU1311 with different combinations of delay and phase in TDM_CFG registers as below:

DLY_EN	PHASE	TDM Configuration
0	0	SLOT0 data MSB is sampled on the first rising edge of BCLK after rising edge of WCLK
0	1	SLOT0 data MSB is sampled on the first falling edge of BCLK after rising edge of WCLK
1	0	SLOT0 data MSB is sampled on the second rising edge of BCLK after rising edge of WCLK
1	1	SLOT0 data MSB is sampled on the second falling edge of BCLK after rising edge of WCLK

NOTE: SLOT0 if SLOT_MAP is 0, SLOT4 if SLOT_MAP is 1.

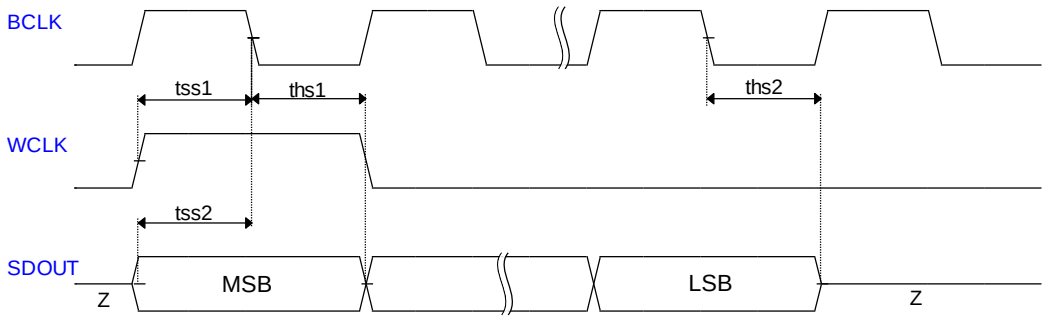
3.2.1 Configuration 1

Both DLY_EN and PHASE in TDM_CFG0 are set to 0. After the rising edge of WCLK (new frame), MSB of SLOT0 is sampled on the first rising edge of BCLK. MSB



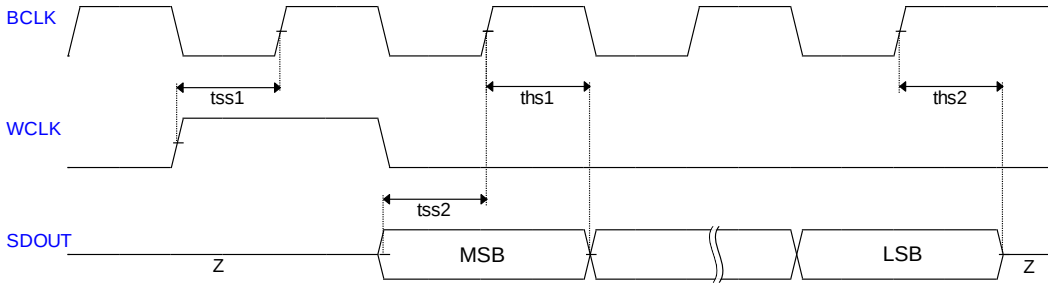
3.2.2 Configuration 2

DLY_EN is set to 0 and PHASE is set to 1. After the rising edge of WCLK (new frame), MSB of SLOT0 is sampled on the first falling edge of BCLK.



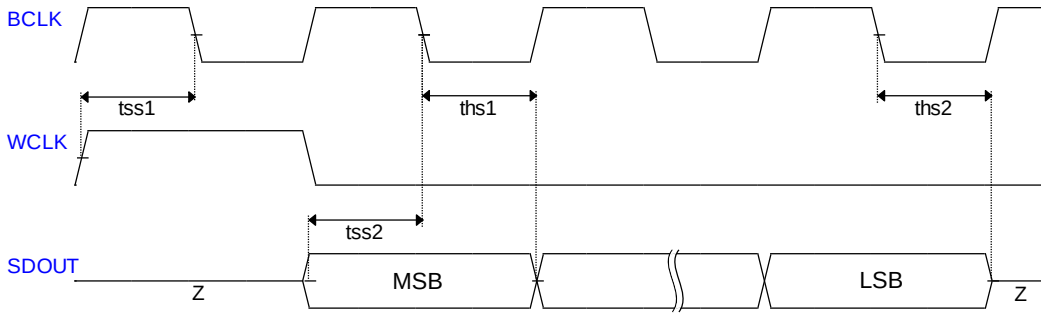
3.2.3 Configuration 3

DLY_EN is set to 1 and PHASE is set to 0. After the rising edge of WCLK (new frame), MSB of SLOT0 is sampled on the second rising edge of BCLK.



3.2.4 Configuration 4

Both DLY_EN and PHASE in TDM_CFG0 are set to 1. After the rising edge of WCLK (new frame), MSB of SLOT0 is sampled on the second falling edge of BCLK.



3.3 TDM frequency

TDM data can be sampled at different rates by configuring BCLK[1:0] in ODR_SEL_BCLK register as below:

00/01: BCLK=1.024MHz, WCLK = 8KHz

10: BCLK = 2.048MHz, WCLK = 16KHz

11: BCLK = 3.072MHz, WCLK = 24KHz

3.4 TDM slot mapping

The slot mapping of axis output data can be configured by SLOT_MAP in TDM_CFG0. Unused slots are in high impedance.

SLOT_MAP	SLOT0	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7
0	X-axis	Y-axis	Z-axis	HiZ	HiZ	HiZ	HiZ	HiZ
1	HiZ	HiZ	HiZ	HiZ	X-axis	Y-axis	Z-axis	HiZ

3.5 TDM max counter

Cmax is the max number of BCLK periods can be contained in a WCLK period. Since BCLK/WCLK ratio is fixed, Cmax is equal to 127 currently (Cmax = BCLK/WCLK – 1).

3.6 Axis configuration

In TDM mode, each axis of accelerometer can be powered down/on respectively by configuring X_EN/Y_EN/Z_EN bits in AXIS_SEL register. If an axis is power down, corresponding TDM data slot is in high impedance.

4. I2C interface

4.1 I2C interface details

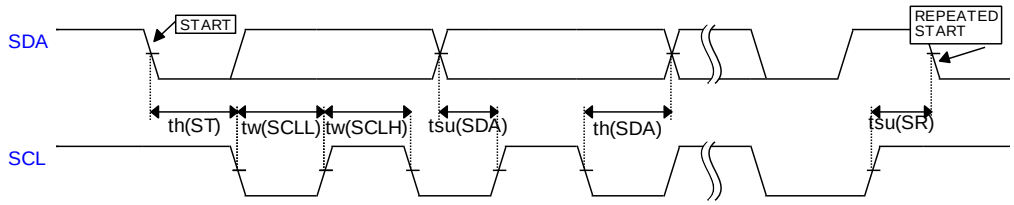
The AU1311 registers can be configured through I2C interface, which is comprised of SCL (serial clock) and SDA (serial data). In addition to SCL/SDA, the AU1311 also provides SA0 for slave address alternation. The I2C data rate of the device is up to 100kbps/400kbps/1Mbps depending on the data transfer modes.

With SA0 low, the 7-bit I2C address is 0x30 followed by the R/W bit. This translates to 0x60 for a write and 0x61 for a read. If SA0 is pulled high, the slave address becomes 0x31 followed by the R/W bit. This translates to 0x62 for a write and 0x63 for a read.

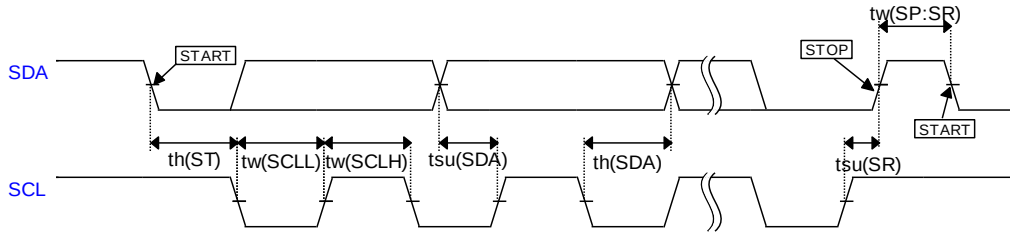
I2C_SA0	Address (7-bit)	R/W bit	Address+R/W (8-bit)	Description
Low	0x30	0	0x60	Write to slave address 0x30.
Low	0x30	1	0x61	Read from slave address 0x30.
High	0x31	0	0x62	Write to slave address 0x31.
High	0x31	1	0x63	Read from slave address 0x31.

4.2 I2C characteristics

Symbol	Parameter	I2C standard mode		I2C fast mode		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{SU(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	μs
$t_{h(ST)}$	START condition hold time	4		0.6		μs
$t_{SU(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{SU(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		



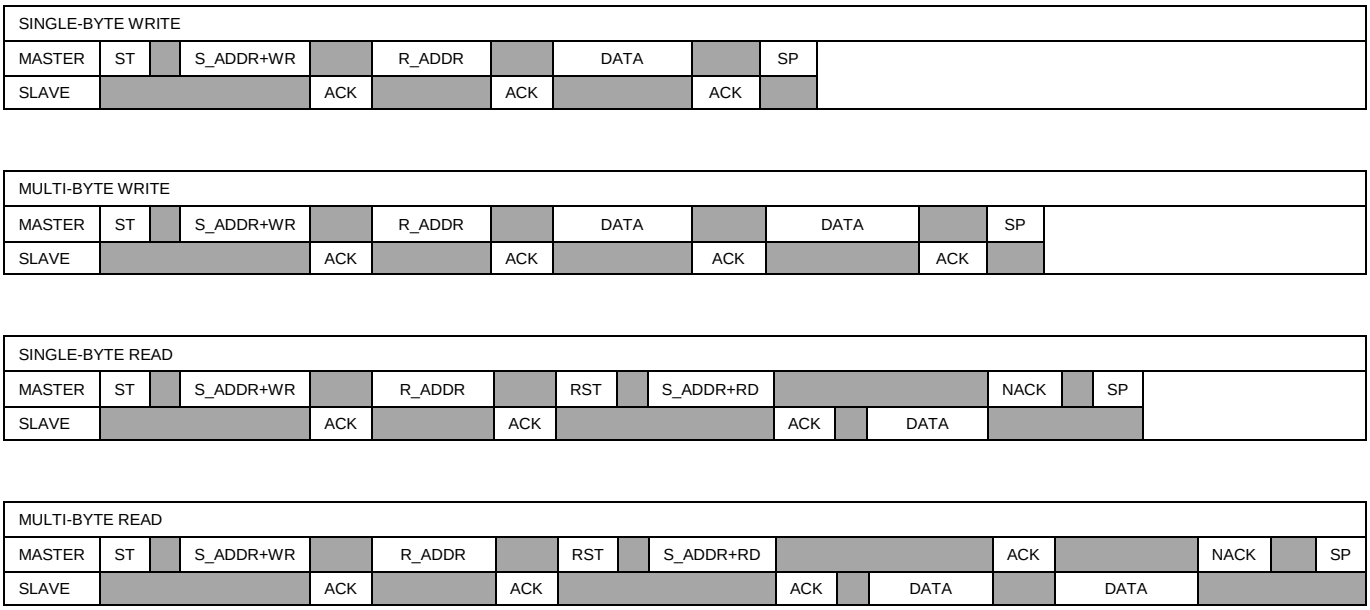
I2C timing diagram 1



I2C timing diagram 2

4.3 I2C read/write sequence

I2C read and write sequences is illustrated as below:



ST: START condition
SP: STOP condition
S_ADDR: Slave address
R_ADDR: Register address
WR: Write
RD: Read
ACK: Acknowledge (SDA low)
NACK: Not acknowledge (SDA high)
RST: Either a restart or a stop followed by a start
Shaded areas represent when the device is listening.

5. SPI interface

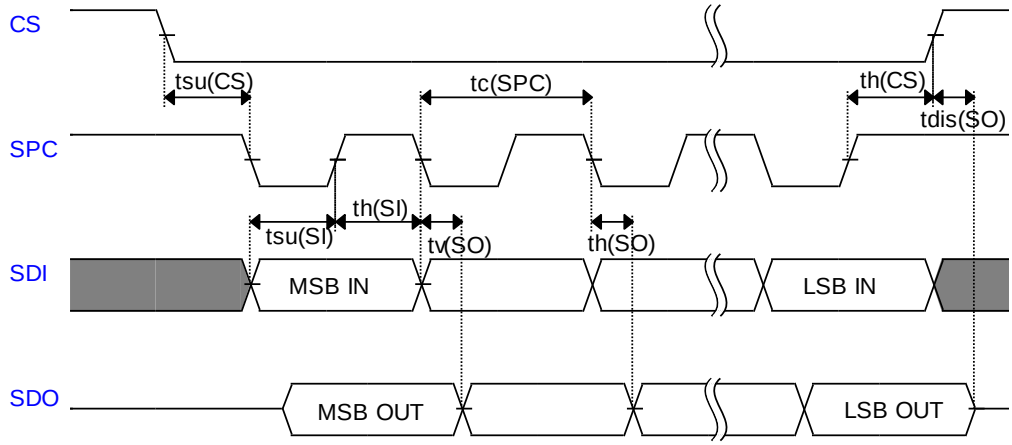
5.1 SPI protocol

The AU1311 registers can also be configured through SPI interface. SPI is a 4-wire interface consisting of SPC(SCL), SDI(MOSI), SDO(MISO) and CS. The master device controls the chip-select line (CS), keeps it low during communication and pulls it high at the end of communication. SPC is the clock signal supplied by master device and is held to high/low if no data transmission. SDI and SDO are serial data input and output.

SPI provides the flexibility to select clock polarity (CPOL) and phase (CPHA) for data synchronization. To communicate with the AU1311, the master device has to set the mode to CPOL=1 and CPHA=1. Clock is high during idle state, data are sampled on the rising edge and shifted out in the falling edge.

5.2 SPI characteristics

Symbol	Parameter	Value		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	20		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	5		
tdis(SO)	SDO output disable time		50	



5.3 SPI command format

The AU1311 provides read and write commands for communication with master device. Data is in 8-bit length and MSB is transmitted first.

Read command:

Bit7	Bit6-Bit0
1	Address of register to be read.

Write command:

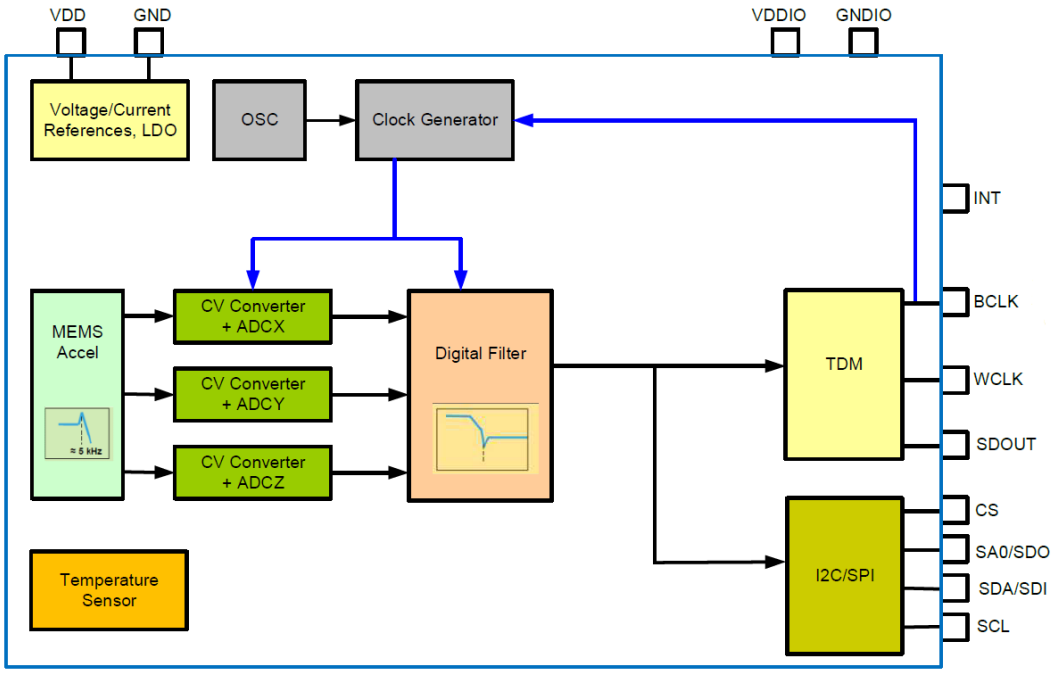
Bit15	Bit14-Bit8	Bit7-Bit0
0	Address of register to be written.	Data to be written to the register.

In the single read/write mode, after the data (8-bit) sent through SDO/SDI, CS signal will go high to end the communication. The AU1311 also provides burst mode to read/write multiple data by one command communication. In burst read mode, a sequence of data from consecutive addresses following the target address will be transmitted automatically through SDO as long as CS is low. In the same way, for burst write mode, a sequence of data to be written to consecutive addresses following the target address can be sent through SDI as long as CS is high.

6. Features

6.1 Electrical architecture

The 3-axis accelerometer's proof mass are driven by a single signal, and 3-axis senses are 3 separate channels. Each channel is implemented as 2nd order ADC with sense capacities integrated inside. With TDM and I2C/SPI interfaces, user can access sensor data by TDM with higher ODR (8/16/24kHz) and SPI with lower ODR (<4kHz) simultaneously, and I2C can be used to configure sensor and system setup.



6.2 Power mode

Upon first applying power to AU1311 or on software reset, the device will enter the standby mode. From standby, the AU1311 can be configured in the various modes as described in the following table:

Mode	Description
Standby	Slow oscillator is on and other circuit blocks are off. Default state upon initial power up or after a reset. Typical current is 1.6μA.
Normal	All circuit blocks are on, both TDM path and SPI path provide data.
Power down	All functional blocks are switched off to minimize power consumption. Digital interfaces remain on allowing communication with the device. All configuration register values are preserved, and output data register values are maintained. The current in this mode is typically 1.2μA.
Reset	Software reset asserted with power applied.
No power	VDDIO and VDD low

7. Registers

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SOFT_RESET	0x01	RES	RES	RES	RES	RES	RES	RES	SRST
ODR_SEL_BCLK	0x02	RES	RES	RES	RES	RES	BCLK1	BCLK0	RES
POWER_CTRL	0x03	RES	RES	RES	RES	RES	RES	PWR_MODE1	PWR_MODE0

TDM_CFG0	0x05	DLY_EN	PHASE	SLOT_MAP	RES	CMAX11	CMAX10	CMAX9	CMAX8
TDM_CFG1	0x06	CMAX7	CMAX6	CMAX5	CMAX4	CMAX3	CMAX2	CMAX1	CMAX0
AXIS_SEL	0x6E	RES	X_EN	Y_EN	Z_EN	RES	RES	RES	RES
CHOP_CTRL	0x6F	CHOP_OPEN	RES	RES	RES	RES	RES	RES	RES
FS_SEL	0x74	RES	RES	RES	RES	FS1	FS0	RES	RES

NOTE: RESERVED bits must remain default value.

8. Register description

8.1 SOFT_RESET (0x01)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RES	RES	RES	RES	RES	RES	RES	SRST

SRST	By writing 1 to this bit, reset the rest of registers and digital circuits (I2C excluded). When soft-reset done (around 20ns), the bit returns to 0 automatically.

8.2 ODR_SEL_BLCK (0x02)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RES	RES	RES	RES	RES	BCLK1	BCLK0	RES

BCLK[1:0]	TDM WCLK/BCLK frequency. Default value: 01. 00/01: BCLK=1.024MHz, WCLK=8KHz 10: BCLK=2.048MHz, WCLK =16KHz 11: BCLK=3.072MHz, WCLK =24KHz

8.3 POWER_CTRL (0x03)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RES	RES	RES	RES	RES	RES	PWR_MODE1	PWR_MODE0

PWR_MODE[1:0]	Power mode selection. Default value: 00.

	00/11: standby mode 01: normal mode 10: power down mode

8.4 TDM_CFG0 (0x05)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DLY_EN	PHASE	SLOT_MAP	RES	CMAX11	CMAX10	CMAX9	CMAX8

DLY_EN	TDM delay mode configuration. Default value: 0. 0: TDM no delay mode 1: TDM delayed mode
PHASE	TDM phase configuration. Default value: 0. 0: TDM data sampled on rising edge of BCLK 1: TDM data sampled on falling edge of BCLK
SLOT_MAP	TDM data slot mapping configuration. Default value: 0. 0: X/Y/Z data mapped to SLOT0/1/2 1: X/Y/Z data mapped to SLOT4/5/6
CMAX11-CMAX8	See TDM_CFG1.

8.5 TDM_CFG1 (0x06)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CMAX7	CMAX6	CMAX5	CMAX4	CMAX3	CMAX2	CMAX1	CMAX0

CMAX[11:0] (combined with TDM_CFG0)	TDM counter max value configuration. Currently, it is fixed to 127. (Cmax = BCLK/WCLK - 1). Default value: 0.

8.6 AXIS_SEL (0x6E)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RES	X_EN	Y_EN	Z_EN	RES	RES	RES	RES

X_EN	Each axis of accelerometer can be powered down/on. Default value: 0.

Y_EN Z_EN	0: power on 1: power down

8.7 CHOP_CTRL (0x6F)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CHOP_OPEN	RES	RES	RES	RES	RES	RES	RES

CHOP_OPEN	Open chopper to reduce noise. Default value: 0. 0: close chopper 1: open chopper

8.8 FS_SEL (0x74)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RES	RES	RES	RES	FS1	FS0	RES	RES

FS[1:0]	The range of full-scale input. Default value: 11. 00: ±2g 01: ±4g 10: ±8g 11: ±16g

Revision history

Date	Version	Changes
	v0.1	Initial release