AU8530: Power Line Smart AC Switch Controller

General Description

The AU8530 is a patented high voltage AC switch controller ~~device~~ that monitors incoming line voltage to ensure that the downstream load only runs at its safe maximum continuous voltage ratings. In the case of an over-voltage line scenario, the AU8530 will shut the AC switch to safeguard and isolate the load, thereby decreasing the possibility of catastrophic failure.

During the recovery time~~r~~ interval (which the user can adjust with an external timing capacitor), normal load operation will resume in the subsequent cycle and be aligned to zero Line-to-Load voltage condition. This results in minimal in-rush current stress And this process continues until the line voltage has stabilized back within safe operating range.

The AU8530, with a 16 V output drive, is the optimal control device for any kind of competitively priced IGBT. Furthermore, to accommodate a broad range of applications, the device is also packaged in a handy compact form factor SOIC-8.

Features

- User adjustable maximum load voltage
- Timing pin for programmable recovery delay
- Line-to-Load voltage monitoring
- Low energizing current 60 µA (typical)
- 'In-cycle' Over-Voltage load isolation
- Suitable for use with IGBT AC switch
- Zero-volt (Line-to-load) AC switch connect
- Zero-volt (Line-to-load) AC switch disconnect
- Compatible with 50 Hz/240 V and 60 Hz/110 V
- Output gate drive voltage of 16 V
- Line to Neutral voltage monitoring
- SOIC 8-pin package

Applications

- White Goods, Home Appliances
- Motor Control & Protection
- Air Conditioners
- Delicate Electronics
- Servers and Data Routers

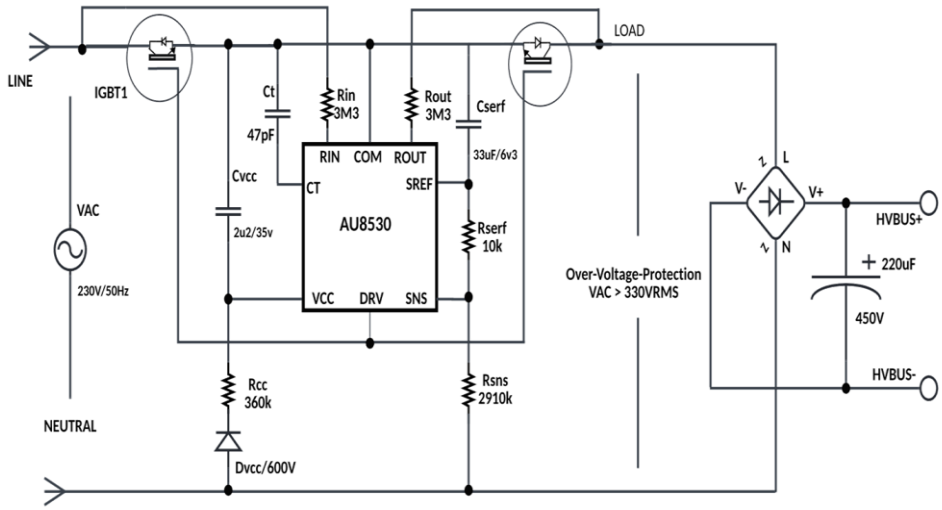

Figure 1 AU8530 Typical Application Diagram

Table of Contents

List of Tables

List of Figures

1 Pin Configuration

1.1 Pin Configuration Diagram

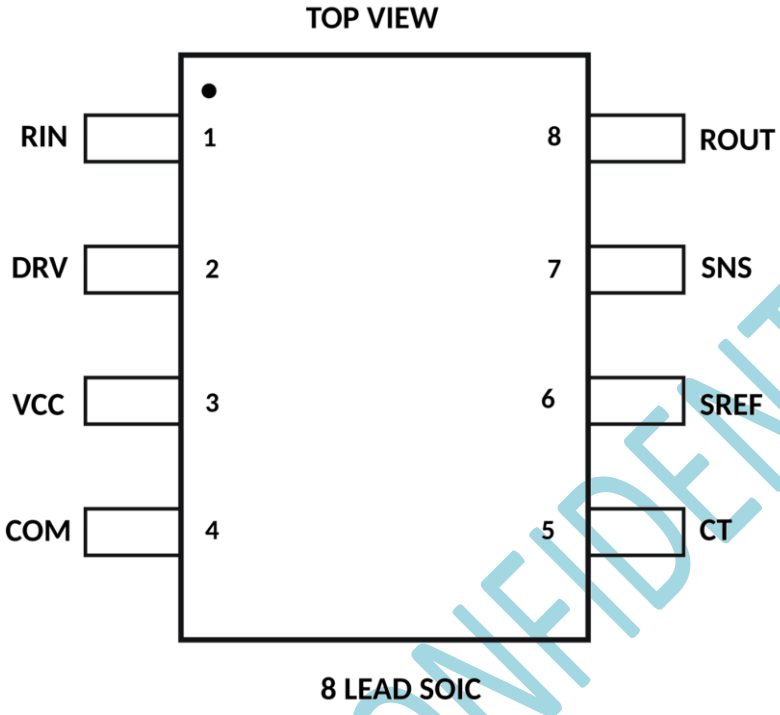

Figure 2 AU8530 Pin Configuration

1.2 Pin Description

Table 1 AU8530 Pin Description

Pin Name	Pin No.	Description
RIN	1	Positive sense input for line-to-load monitor (external resistor to Line side)
DRV	2	Output driver to control IGBT gate
VCC	3	Supply bias voltage input
COM	4	Ground reference point for all voltages (connect to IGBT common emitter point)
CT	5	Restart timing delay control (external capacitor to COM pin)
SREF	6	Sense reference pin for Line-Neutral monitor (connect with 33 µF capacitor to COM pin and 10 K resistor to SNS pin)
SNS	7	Sense input voltage for overvoltage monitoring (external resistor to Neutral)
ROUT	8	Negative sense input for Line-to-load monitor (external resistor to Load side)

2 Electrical Characteristics

Table 2 Absolute Maximum Ratings[1]

Parameter	Pin	Min	Typ	Max	Units
Power Supply	VCC, DRV	-0.3		20	V
	RIN, ROUT, CT, SNS, SREF	-0.3		5.5	V
Clamping Current	VCC to COM	0		20	mA
	RIN, ROUT, SNS	-2		2	mA
Operating Junction Temperature		-40		150	°C
Storage Junction Temperature		-65		150	°C
MSL Level		MSL 1			

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to- ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX) = (T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Peak bias current into V_{CC} pin[1]	I_{CC} Peak	0		10	mA
V_{CC} bias resistor	R_{CC}	100		360	kΩ
V_{CC} bypass supply capacitor	C_{VCC}	2.2		3.3	µF
S_{REF} Resistor	R_{SERF}	9		11	kΩ
Sense reference filter capacitor	C_{SERF}	22		47	µF
Line-Load sense resistors	R_{IN}/R_{OUT}	2.2		3.3	MΩ
DRV pin load capacitance	$DRV_{C\text{-}LOAD}$			30	nF
Ambient Operating Temperature	T_{AMB}	-40		105	°C

Notes:

1. I_{CC} peak current applies to worst case maximum continuous VAC peak voltage: (VAC peak voltage -18V)/R_{CC}

Table 4 Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
V_{CC} UVLO	Rising Condition (V_{CC} OK)	13.8	14.6	15.4	V
	Falling Condition (V_{CC} Fault)		13.3		V
	Hysteresis Condition (V_{CC} OK, Fault)		1.3		V
V_{CC} CLAMP	I_{VCC} =1 mA		17.6		V
	I_{VCC} =10 mA		18.2		V
$I_{ENERGIZE}$	I_{VCC} Startup Current (min)	40	60	80	µA rms
$T_{ENERGIZE}$	VAC = 230 V RMS 50 Hz (start- up time)		0.4		sec
V_{SERF}	Regulated voltage in normal condition	-5%	2.0	+5%	V
$V_{STARTMAX}$[1]	| V_{SNS}-V_{SREF} | absolute	-6%	1.5	+6%	V
OVP_{TRIP}[2]	| V_{SNS}-V_{SREF} | absolute	-5%	1.6	+5%	V
T_{CT}	1 nF from CT to COM (timing delay)		0.8		sec/nF
I_{CT}	Source/Sink Current (timing current)	6	9	12	µA
T_{DRV_HI}	10 % to 90 % (high rise timing)		6		µs
DRV_{LO}	IGBT gate discharge (sink current)		20		mA
DRV_{ROL}	DRV < 0.6 V (off state resistance)		10		Ω
RIN_{CL}	I_{RIN} = ± 1 mA (clamp voltage)	0.3		4.4	V

Parameter	Conditions	Min	Typ	Max	Units
$ROUT_{CL}$	I_{RIN} = ± 1 mA (clamp voltage)	0.3		4.4	V
SNS_{CL}	I_{SNS} = ± 1 mA (clamp voltage)	0.3		4.4	V
I_{LEAK_RIN}	-40 mV < V_{RIN} <+40 mV (leakage current)	-0.05	0	0.05	µA
I_{LEAK_ROUT}	40 mV < V_{ROUT} <+40 mV (leakage current)	-0.05	0	0.05	µA
I_{LEAK_SNS}	+0.2 V < V_{SNS} <+3.8 V (leakage current)	-0.05	0	0.05	µA
$TSD_{JUNCTION}$	Drive pin low		150		°C
TSD_{HYST}			25		°C

Notes:

1. VAC peak input voltage for figure 1 circuit load startup = $V_{STARTMAX}$ * (R_{SNS}+R_{SERF}) / (R_{SERF}) peak = ~ 438 Vpk = ~310 V RMS
2. VAC peak input voltage for figure 1 load isolation = OVP_{TRIP} * (R_{SNS}+R_{SERF}) / (R_{SERF}) peak = ~ 467 Vpk = ~330 V RMS

Table 5 ESD Ratings

Parameter	Value	Units
Human Body Model (HBM), per Joint JEDEC/ESDA JS-001-2017	±2	kV
Charged Device Model (CDM), Joint JEDEC/ESDA JS-002-2018	±1	kV
Latch-up Immunity, JESD78E, Class 2, +125 °C	±100	mA

Table 6 Thermal Characteristics

Thermal Resistance	θ_{JA}	θ_{JC}	Units
SOIC-8	170		°C /W

3 Functional Description

The AU8530 is an AC switch controller that instantly cuts off incoming AC power in the event that imminent over voltages are detected, thereby preventing the load from being sustained above its maximum ratings

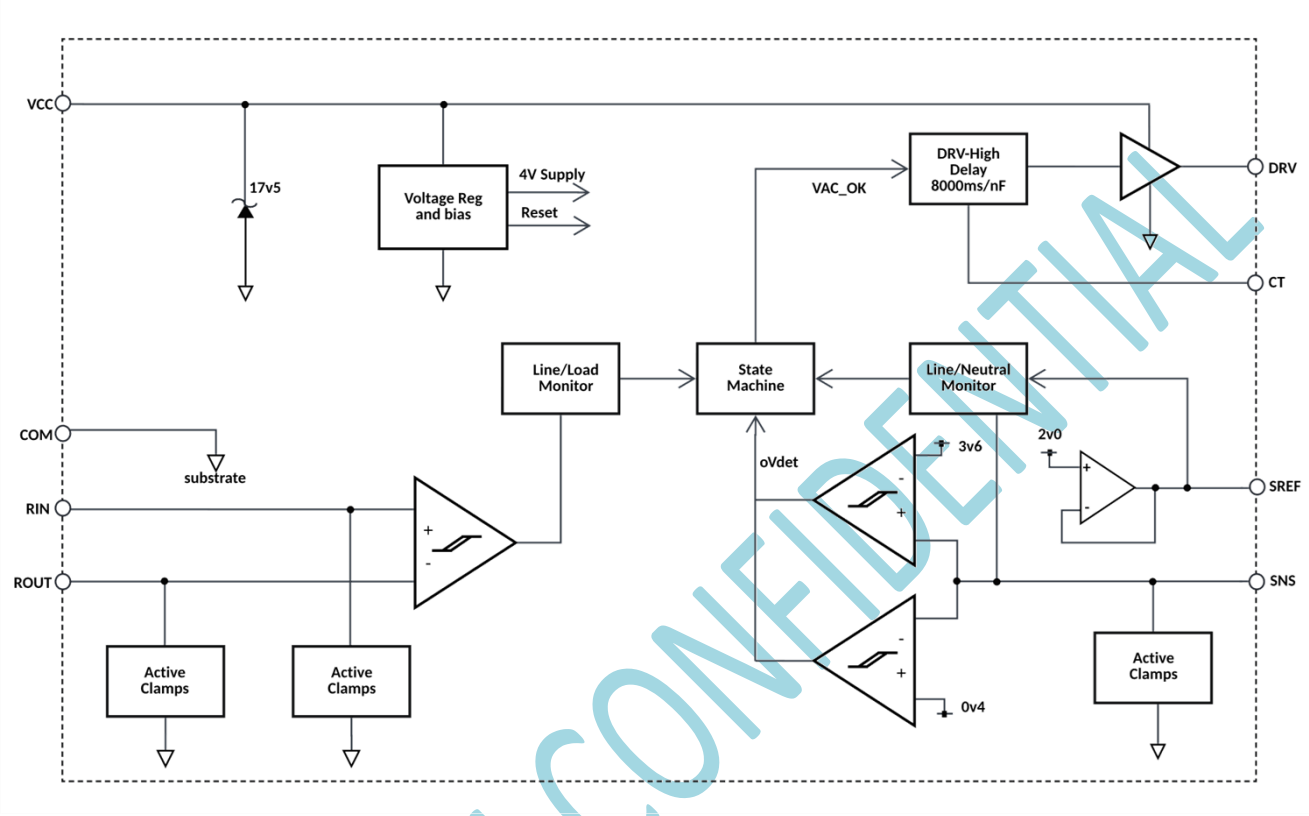

Figure 3 Functional Block Diagram

The load is reconnected and regular functioning begins after the incoming AC power voltage has leveled to values that are safe. The 'connect/disconnect' function of the AC switch is always synced to the OV (zero volt) Line-to-load state, which prevents excessive in-rush currents and inductive "kick-back" spikes. The external component values, CT and RSNS, let the user to alter the stabilization timer interval (CT delay) and over-voltage protection (OVP) level.

3.1 VCC PIN

The supply bias voltage, or V_{CC} pin, of the AU8530 has an undervoltage lockout circuitry (UVLO) built-in to prohibit activation until sufficient voltage is present to run the external IGBTs. The device can start operating normally when the typical input supply bias current exceeds UVLO, which is only 60 μA rms. With the component values (R_{CC} of 360 k) displayed in Figure 1, the UVLO level can be reached at about 60 V rms of VAC input.

Selecting alternative, higher or lower, values for R_{CC} bias resistor will accordingly adjust the nominal VAC input voltage at which the UVLO level is achieved. Any additional Icc current injected into the Vcc pin will be safely clamped once V_{CC} rises to 17.5 V. The peak V_{CC} pin current is recommended to be less than 10 mA.

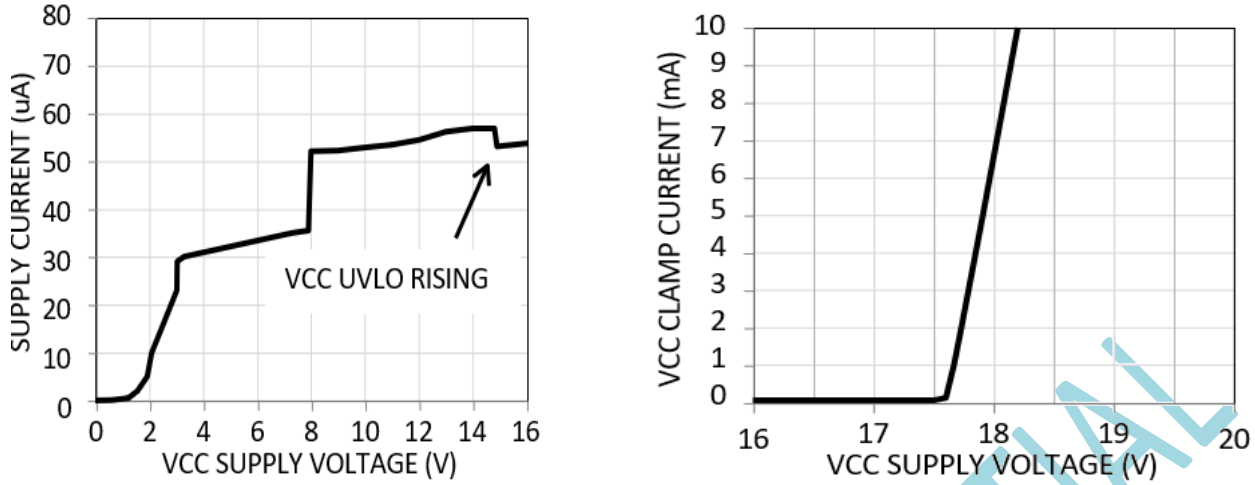

Figure 4 VCC Operating and Clamping Current

3.2 SERF PIN

For the purpose of providing a precise AC reference for detecting over-voltage events, the S_{REF} pin has an inbuilt 2 V regulator. The external resistor (9 kΩ ~ 11 kΩ range) connected to the SNS pin and an external capacitor (22 µF ~ 47 µF range) connected to the COM pin are needed for the S_{REF} pin.

There is a slight offset shift from the nominal Over Voltage Protection (OVP) goal setting as a result of the 2 V bias reference at the S_{REF} pin. Generally, negative OVP events will cause 2 V to be raised, and positive OVP events will cause 2 V to be lower than the design target. At OVP settings of around 330 V rms (267 V peak), the deviation from the nominal design desired result is less than 0.5%.

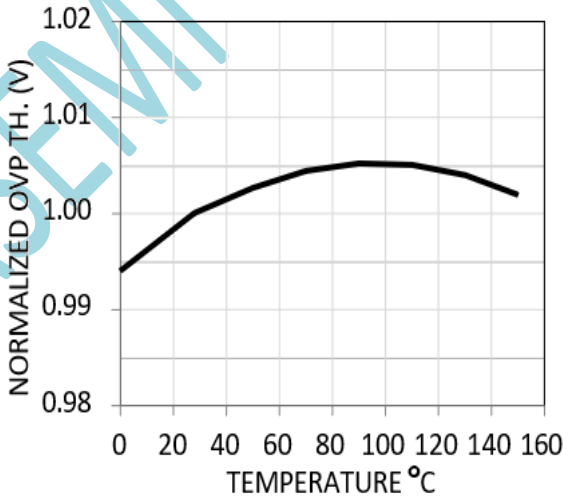

Figure 5 Normalized OVP Threshold Vs Temperature

3.3 RIN/ROUT PINS

The circuitry required to detect the zero-voltage situation across the AC switch—which synchronizes the AC switch turn-on/off events—is contained in the R_{IN}/R_{OUT} pins. Furthermore, active current clamp circuitry is incorporated into both R_{IN}/R_{OUT} pins to guarantee that their voltage levels remain within safe working limits.

When the AC switch is in the off position, the maximum current clamping level into either pin happens at the VAC peak positive phase for the R_{IN} pin and the VAC peak negative phase for the R_{OUT} pin.

To enable the system to manage VAC peak voltages above 2 kV, external resistor values for R_{IN}/R_{OUT} resistors should be set within the range of 2.2 MΩ to 3.3 MΩ when current clamping levels exceed 1 mA. When 3.3 MΩ external resistors are employed, the pin capacitance of R_{IN} and R_{OUT} is approximately 5 pF, resulting in a time constant delay of around 15 μs.

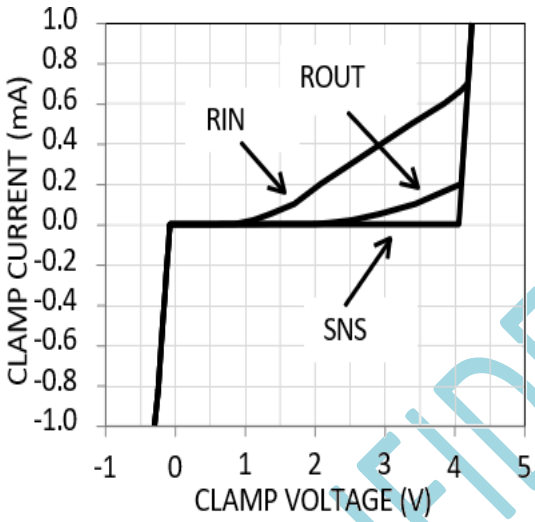

Figure 6 RIN/ROUT/SNS Clamp Current

3.4 SNS PIN

The SNS pin serves as the input voltage for over-voltage protection and is connected to the S_{REF} pin by a nominal resistor with a value of 10 kΩ. The AC-switch turn-on procedure begins when the peak voltage differential between SNS and S_{REF} falls within ±1.5 V during initial start-up or over-voltage recovery.

When the device is in normal operation, with AC-switch turned-on, an over-voltage event will be detected if the peak voltage difference between SNS and S_{REF} exceeds the range of ±1.6 V (i.e. SNS input voltage exceeds 3.6 V or falls below 0.4 V), at which point the AC switch is turned-off upon the next O V Line-to-load event. A phase positive over-voltage event, will turn-off the AC- switch on the falling edge of Line-to-load zero voltage and a negative phase over-voltage event will turn-off the AC-switch on a rising edge of Line-to-load zero voltage.

$$\text{Start-up VAC peak} < 1.5\text{V x } (\text{Rsns} + \text{Rsref})/\text{Rsref (V)}$$

$$\text{OVP trip VAC peak} > 1.6\text{V x } (\text{Rsns} + \text{Rsref})/\text{Rsref (V)}$$

For the component values as shown in Figure 1, this equates to:

$$\text{Start-up VAC peak } < 1.5\text{V x } 2920\text{k}/10\text{k} = 438\text{ (V)} < 315\text{V RMS}$$

$$\text{OVP trip VAC peak} > 1.6\text{V x } 2920\text{k}/10\text{k} = 467\text{ (V)} > 330\text{V RMS}$$

The SNS pin input also contains internal active current clamping circuitry in the event of extreme over-voltage conditions that can safely clamp current level in excess of 1 mA.

3.5 CT PIN

By using the CT pin, the user can program a timing interval (CT delay) during which the VAC voltage needs to be kept stable and below the maximum start-up voltage. Following one complete cycle in which the VAC is inside the start-up voltage range, the timer starts to run. This holds true for OVP recovery as well as the initial power-up state. The total timer duration is set via an external capacitor placed between the CT pin and the COM pin.

The CT timing circuitry progressively ramps the external capacitor between 3.7 V and 0.3 V and back to 3.7 V through an internal pull-down current of 9 μA and an external pull-up current of 9 μA. During 1024 cycles, this sequence yields an overall timer coefficient of 0.8 sec/nF.

$$= 1024 \text{ x } 3.4 \text{ x } 2 \text{ x CT (F)} / 9\text{u} = 0.774 \text{ sec/nF}$$

Following the completion of the timer interval, the AC switch will be synchronized to activate at the subsequent zero voltage rising edge of the Line-to-load voltage.

When VAC goes beyond its permitted start-up voltage during the timer interval, the timer will be reset and wait for the next full cycle in which VAC is back within its start-up voltage before it is reactivated.

3.6 DRV PIN

The AU8530's DRV pin provides the voltage required to sufficiently operate the external high voltage back-to-back IGBTs that make up the AC switch. An Nfet "voltage follower" in the internal circuitry drives the output to within 0.75 V of the V_{CC} voltage. The DRV voltage output will likely proceed to 17.5 V during severe V_{CC} current clamping conditions and fall to 13 V when the V_{CC} level returns to UVLO.

It's not necessary to run the IGBTs very quickly because the AC switch's on/off function is always coordinated with its zero-voltage state.

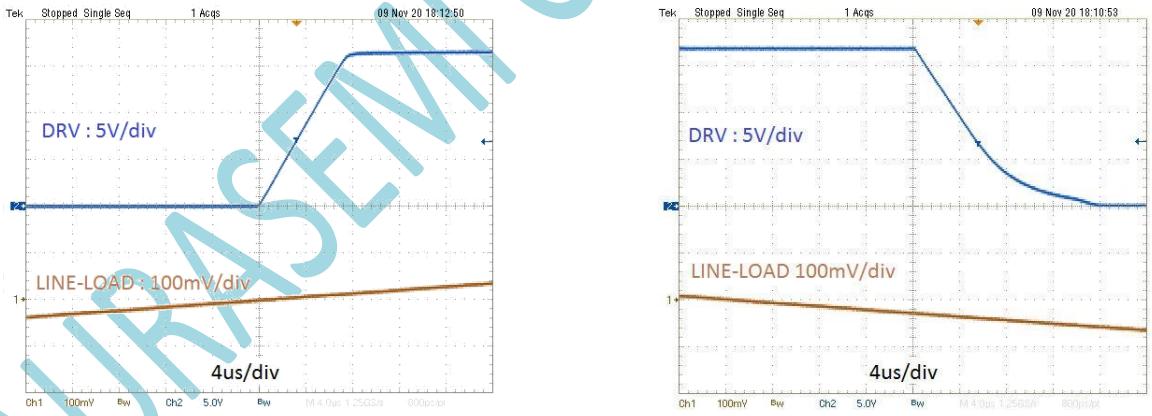

Figure 7 DRV Transient Turn On/Off (10 nF Load)

The DRV output ramps smoothly across a 6 μs time interval for IGBT turn-on events, regardless of the external capacitive load. In order to safely drive IGBTs into their "off" state within 8 seconds, the DRV pin discharges via a 20 mA current sink during IGBT turn-off events. At that point, 10 Ω internal pull-down is triggered when the DRV voltage drops below 0.6 V.

Reverse current from the DRV pin to the V_{CC} pin can also travel through an internal power diode in the DRV circuitry. This makes sure the DRV voltage output will always be low enough to avoid IGBT turn-on situations during the AU8530 first power-up, while V_{CC} is still or almost O V.

4 Thermal Dissipation

The AU8530 thermal dissipation is primarily determined by the levels of V_{CC} clamping current.

A half-sine wave with a maximum peak current of 10 mA is the clamping current into V_{CC} under the maximum parameters shown in Table 3, with the ambient operating temperature being +105 °C. An average clamping current of 3.75 mA (50% x 10 mA / √2) would equal the VCC voltage, which would normally be 18 V.
It will dissipate power on average of:

$$\text{Pdiss} = 18\text{V x } 3.75\text{mA} = 68\text{Mw}$$

Using the SOIC-8 package junction to ambient thermal resistance (ThetaJA) of 170 °C/W, the resulting junction temperature with 68 mW dissipation at +105 °C ambient would be:

$$\begin{aligned}\text{Tjunct} &= \text{Pdiss x ThetaJA} + \text{Tambient}\\ &= 68\text{mW x } 170\text{°C /W} + 105\text{°C}\\ &= 12\text{°C} + 105\text{°C} = 117\text{°C}\end{aligned}$$

When the junction exceeds 150 °C, an exceptional case of thermal overload occurs, in which case the load is separated at the next Line-to-load zero voltage event falling edge. The standard start-up procedure will begin instantly as the junction temperature drops below 125 °C once more.

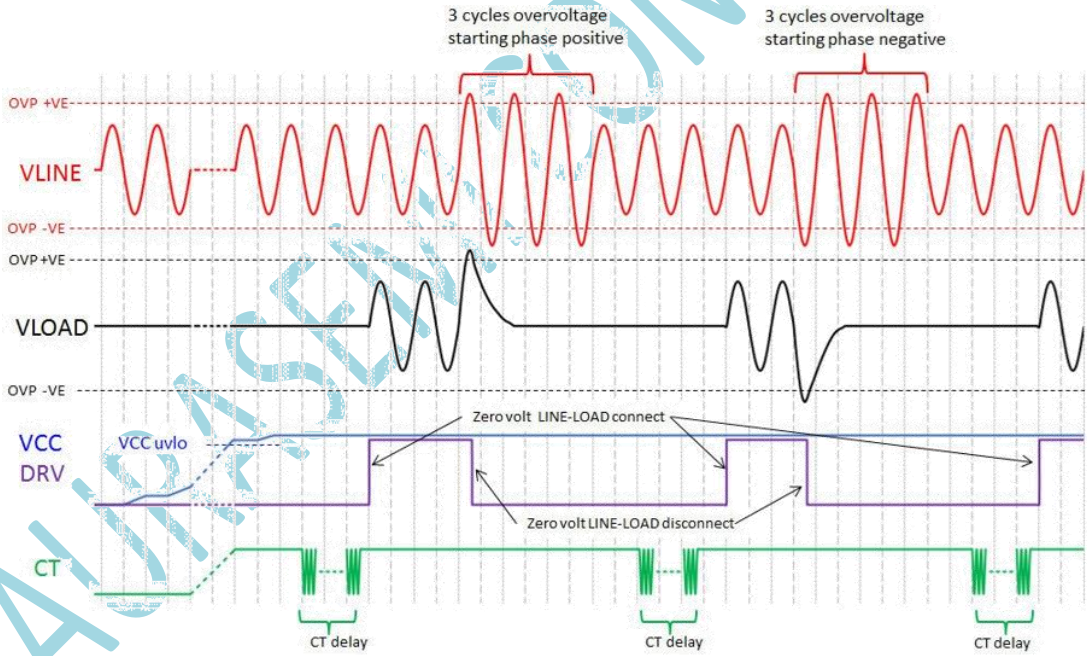

Figure 8 Over-Voltage Protection Timing Example

5 Package Description

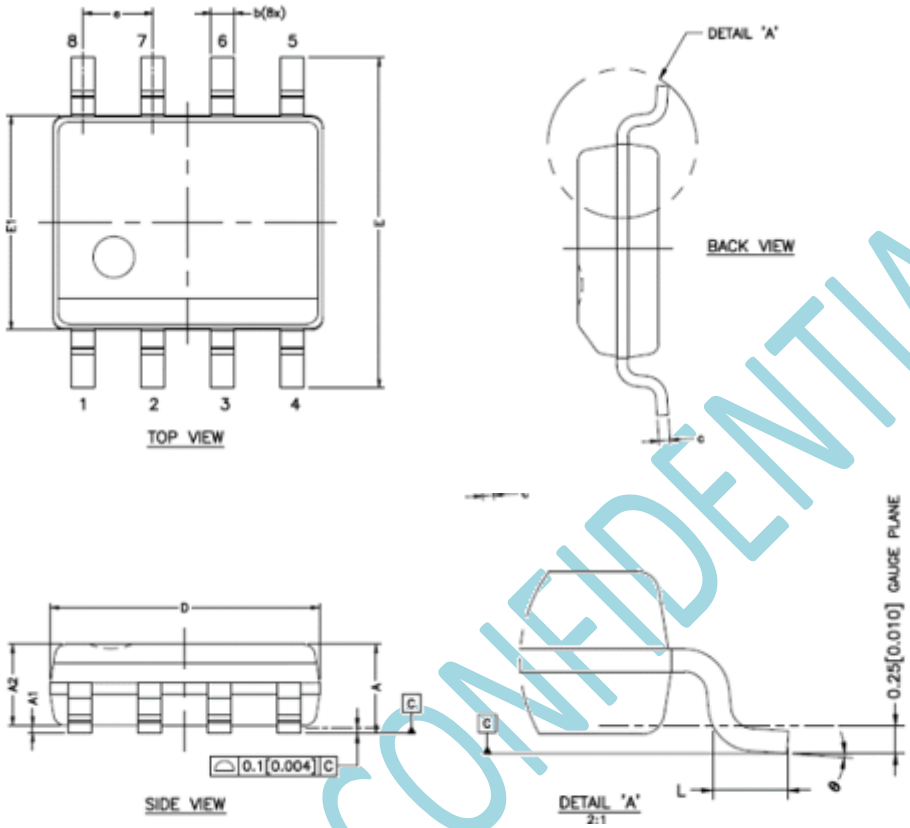

Figure 9 AU8530 SOIC 8

Symbol	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.50	0.049	0.059
b	0.35	0.49	0..014	0.019
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050
θ	0º	8º	0º	8º

Note: All dimensions shown are in millimetres (mm) unless otherwise noted.

6 Ordering Information

Table 7 AU8530 Ordering Information

Ordering Part Number (OPN)	Marking	Package information	Temperature Range	MSL
AU8530	AU8530	SOIC-8	-40 °C to 105 °C	1

Note: This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

6.1 Top Marking

TBD

Figure 10 AU8530 Top Marking

7 Revision History

Table 8 Revision History

Version Number	Date	Description	Author
1.0	28th Aug 2024	AU8530 Datasheet created	Aurasemi

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