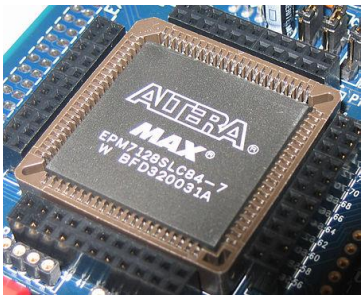
ASIC, CPLD, FPGA Migration is not a Flight of Fancy

Whether it is progress or economic pressures that is behind the reality of discontinued ASIC, CPLD or FPGA packages a cost effective, Triple F (form, fit and function) solution is not that far away.

As the trend for extended product life continues to become more popular, the product development and the mid-life improvement programmes of electronic equipments are quickly vanishing into the future.

The environment the adapter will be applied to is considered at the beginning of the enquiry/design to ensure accurate compliance to critical elements and we will work very closely with you in that respect. When appropriate, we will adopt DO254 guidelines for the design assurance of electronic hardware in airborne systems. The robustness of the adapter program has been proven over three decades in harsh environments including Civil Aerospace, Defence (air, land & sea), Rail (rolling stock & trackside), Oil & Gas (deep drilling & infrastructure).

One advantage of using an adapter to migrate to new, available technology is that during the design special requirements can be incorporated. Quite often the new design can provide product improvement as well as solving supply issues and the adapter route offers an excellent platform for this to be undertaken.



Issues commonly occur during procurement of the extended life product when devices such as ASICs (application specific integrated circuits), CPLDs (complex programmable logic devices) and FPGAs (Field Programmable Gate Array) are involved, and this inevitably means a bounce back to the design engineer's desk from procurement when the original device cannot be found.

An Altera MAX 7000-series CPLD with 2500 gates.

However, as these devices are software configurable, their with currently available similar devices becomes a relatively easy once, the software required becomes the easier of the tasks to The development environments and design software now support these new devices permit code development, testing to be achieved with ease.

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The challenge of Integrating the new hardware into an existing design, a design which was created several years ago using, what was then, cutting edge technology but now considered archaic, can be overcome with the right choice of component and the adherence of some simple guidelines. In most cases there are two areas which need to be considered, the choice of new component and the design of an interface (adapter) which is generally required for successful integration into the old design.

Future Proofing the Design

It is possible to take this concept a stage further whilst recognising the skill sets required by different design blocks. If the core processing element of a board can be separated and concentrated on an adapter/daughter board using an FPGA and associated circuitry then future component supply problems can be simply eliminated as this element can be continually refreshed and replaced. In this instance re-targeting the design is a relatively simple operation so long as industry standard coding techniques and languages have been used along with industry standard interfaces. This technique can have some interesting cost benefits as usually it is only the intelligent core of the design which requires a high PCB layer count and the area of the expensive board is greatly reduced.

Device Selection

So, what needs to be considered when selecting a FPGA to replace an ageing logic design if it is to integrate into the existing design with the minimum of disruption?

The functional capability of the new device is solely determined by the complexity of the original design. The point to note is that the device needs only to have the capability to meet the *original* design requirements and NOT the requirements of the original device. In many cases the original device has a far greater capability than was required originally required for the design, especially with respect to I/Os. Generally, if the new device is matched to the design requirement then the resultant interface design can be considerably easier. If the new device does have spare signals, then consideration must be given as to what to do with them. Recommendations of some manufactures mean that spare I/Os need to be tied to a specific level whereas others can be left open circuit. The resultant design and power implications can be considerable if a significant number of spare I/Os need to be terminated.

Speed

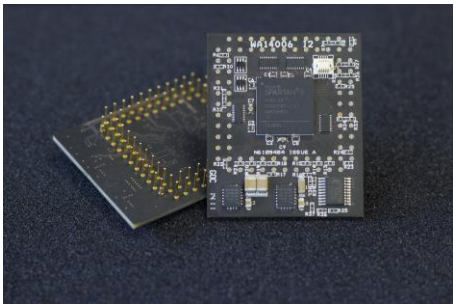
The speed of any replacement device will undoubtedly be far superior to the original used due to improvements in current manufacturing techniques. However, the question should be asked as to whether the rest of the design can handle these increases in response and access times. Usually delays can be incorporated within the software of the new design, but it does need to be considered at the selection stage as not all devices can provide this type of code. Physical delays can be incorporated as part of the adapter design but are not recommended as a rule.

Code Storage

A lot of existing ASIC and CPLD devices do not contain on chip memory for code storage so this is normally accomplished using a separate memory chip. Although these chips will have sufficient storage, a common problem is the memory's relatively slow access times which can provide several problems for the new device. There are normally three solutions:

1. Abandon the memory chip and select an FPGA with on-board code storage,
2. Incorporate a compatible memory as part of the adapter or
3. Provide an adapter with a faster memory device to replace the existing code storage medium.

Original Adapter design (2002) utilised Xilinx XCS10-3TQ144C & XC17S10V08C. Last time buy announced 2010



Replaced with Xilinx XC6SLX4-2CSG225C & XCF04SVOG20C Adapter used until equipment re-design in 2018

If we are designing with the future in mind it is far better to choose a device with its own storage as this means that when the time comes for the adapter to be re-designed only this device will need to be replaced and not the configuration device as well.

Core Voltage

The selection of the new device need not be constrained by the motherboard operating voltage. It is commonplace nowadays to include circuitry to adjust (usually down but not always) the in-coming voltage to the adapter to match the core voltage level (VccCore) of the new device.

Although it can be a relatively simple job to change the voltage used for the core supply of the new device, careful consideration must be given to the compatibility of the new device to the existing circuitry with respect to I/O levels. The common problem is that the existing design uses TTL levels or even worst CMOS levels, and the new device operates at either 3.3 or even 1.8 volts. Even though the signals can be TTL 'tolerant' where inputs can operate with the existing levels it can mean that the output levels are not high enough to drive the existing circuits. Some devices allow the provision of I/O power levels which are different to the core voltage, and in some cases it can be possible to provide drivers to adjust the new levels to an acceptable level, but it is usually constrained to a small numbers of outputs.

In most cases, no signal types present problems in the design of the interface because with short inter-connect distances even very high speeds can be accomplished. Balanced pairs and matched impedance designs are easily accomplished but need to be identified at design conception as this can influence the whole design. This is especially true with balanced pairs which must achieve equidistant signal paths. Although most input signal will draw very little current care must be taken with certain types of outputs which can draw large currents (large with respect to the rest of the design). These do not present problems but must be indentified early so that correct tracking can be utilized in the design.

De-coupling

The decision needs to be made at design conception as to whether the adapter is to include the de-coupling devices for the new device, whether the existing de-coupling capacitors on the motherboard can be utilized or whether it will be a combination of the two. Much will depend on the existing design. In most cases there is sufficient de-coupling on the existing board, especially when the adapter utilizes ground and power planes as part of its design. In these cases, a de-coupled Vcc (voltage common collector) input to the adapter is taken directly to a power plane. In the same manor the device power inputs are also connected directly to the power plane. Only where very little de-coupling on the motherboard has been provided or where the adapter does not utilize power planes should consideration be given to other de-coupling techniques.

Physical Size

It is generally a design requirement that the adapter design be no larger in area than the existing device. If this constraint is not applicable consideration will have to be given as to how the adapter is soldered onto the motherboard. If all interconnects cannot be accessed by a soldering iron, then all the adapters (including those used in development for design proving) will have to solder using reflow. However, constraints in the Z axis are not generally a problem as the adapter can utilize PoP (package on package) type techniques to provide additional surface area. Of course, the size required will be directly proportional not only the size of the chosen FPGA but the ancillary circuits which will have to be included as part of the new design, i.e. power supply, interface matching etc.

Environment

Although temperature, humidity and acceleration can provide constraints to design, the main factor which should be considered at design conception is vibration. The use of printed circuit substrates which are the same to the motherboard (with respect to coefficients of expansion) means that high LLC inter-connect techniques can be utilized without experiencing the reliability problems associated with those devices which use that inter-connect method. This will result in the adapter having a very low centre of gravity with respect to the motherboard and thus minimizing the effects of vibration.

Programming

The inclusion of the ability to program on board either the FPGA and or the memory chip is a desirable provision. This may have been impossible with the original design, but the change of memory device and the introduction of a FPGA will undoubtedly change the method. The more modern types of programming interface are more desirable as they tend to use less circuits i.e. ST Micro SWIL as opposed to JTAG.

This solution will provide a fast, cost effective bridge, a means of travelling across the void left by component unavailability to a time when the problem can either be resolved by re-design or product replacement. But what if this concept of bridging was applied at initial design conception? Could it be possible for foundations to be left in designs for future bridges to be built across critical components? If it could, future obsolescence problems may be solved with greater ease and the phrase pro-active obsolescence management would be nearer to a reality.

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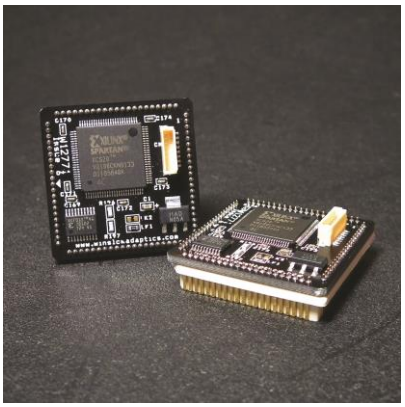
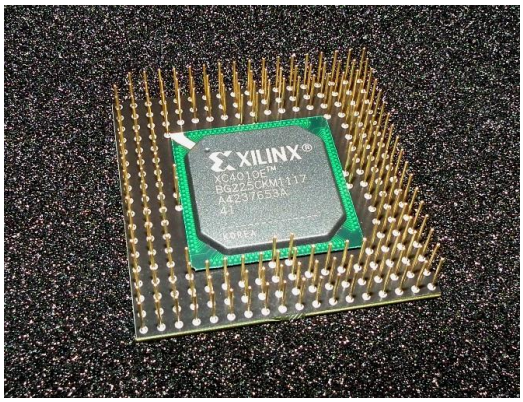
Adapting from QFP (quad flat pack)



Pluggable PLCC with Jtag



Ensuring the original footprint is maintained


WINSLOW
ADAPTICS