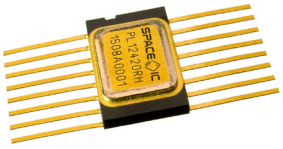


SPPL12420RH

2 A Synchronous Rectified Step-Down Converter

FEATURES

- 2 A continuous output current
- Input voltage capability (derating reference): 24 V
- Minimum input voltage: 4.5 V
- Minimum output voltage: 0.923 V
- Latch-up immune (fully isolated SOI technology)
- Hermetic dual in-line 16-lead flatpack package
- Screened according to ESCC
- High, > 90%, efficiency (V_{IN} = 5 V, 0.25 A < I_{LOAD} < 2 A)
- Fixed 340 kHz frequency for small filter size
- 3 µA (MAX) shut-down supply current
- Programmable soft-start, cycle-by-cycle over-current protection and input under-voltage lockout
- Extended temperature range: -55 °C to +125 °C

DESCRIPTION

The SPPL12420RH is a radiation hardened monolithic synchronous buck regulator featuring integrated 110 mΩ MOSFETs that provide continuous 2 A output load current. Its current mode control circuitry provides fast transient response and cycle-by-cycle current limit.

The SPPL12420RH can be operated at input voltages up to 24 V, which is the derating reference. The SEE-related limitation of the input voltage depends on the target LET level.

The device is packaged in a hermetically sealed 16-pin flatpack with heatsink and straight leads.

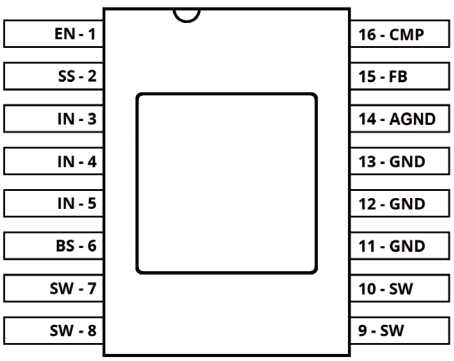
RADIATION HARDNESS

- LDR TID > 40 krad (Si) - biased
- SEL, SEFI and SEU immune
- Free from any destructive SEE at:
  - V_{IN} ≤ 13V, LET ≤ 60 MeV·cm²/mg
  - V_{IN} ≤ 11V, LET ≤ 85 MeV·cm²/mg
- SET-free at LET ≤ 35 MeV·cm²/mg
- No critical SETs at LET > 35 MeV·cm²/mg

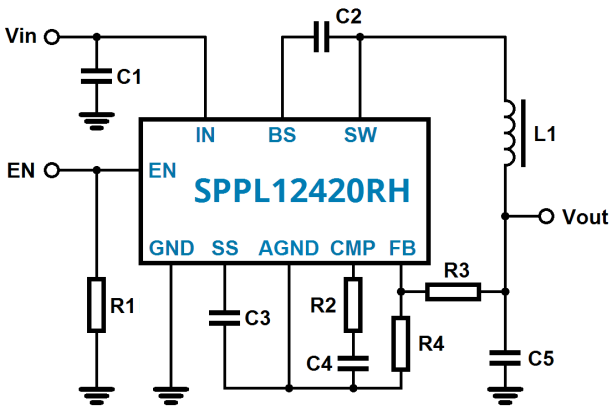
APPLICATIONS

- High-Density Point-of-Load Regulators
- Distributed Power Systems
- Satellite Systems
- Launch Vehicles

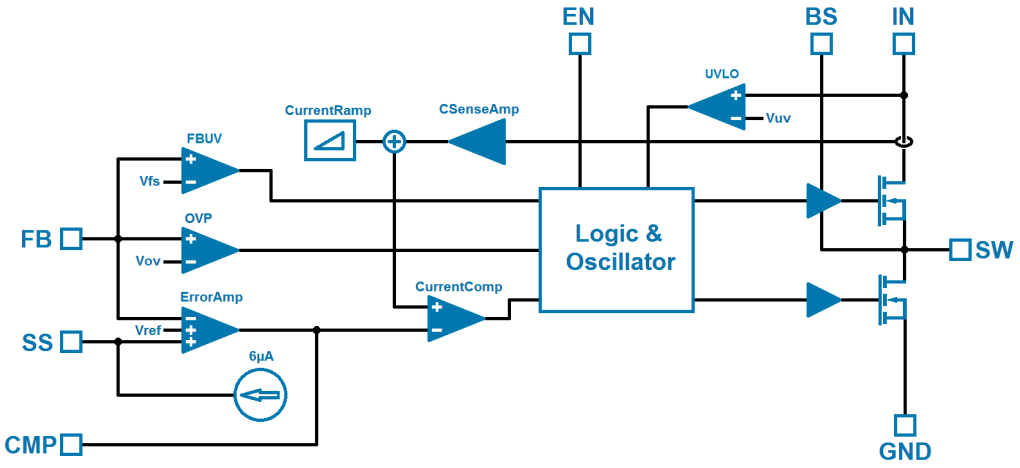
PIN DIAGRAM



TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	PIN DESCRIPTION
EN	1	Enable input pin: The EN pin is a digital input pin that enables or disables the regulator. Set the EN pin high to turn the regulator on; set it to GND, to turn the regulator off. For automatic start up, pull this pin to IN by ≥100 kΩ resistor.
SS	2	Soft-start control input pin: This pin controls the soft-start period. Connect a capacitor from the SS pin to the AGND pin to set the soft-start period. A 0.1 µF capacitor sets the soft-start period to 15 ms. To disable the soft-start feature, leave the SS pin unconnected.
IN	3, 4, 5	Power input pin: The IN pin supplies the input voltage to the internal supply and step-down converter power MOSFETs. Drive the IN pin with a 4.5 V to 24 V power source. Bypass the IN pin to GND pin with an appropriate large capacitor to minimize noise and ripple on the input to the device.
BS	6	High-side gate drive boost voltage input pin: This pin supplies the driver for the high-side N-Channel MOSFET. Connect a capacitor of 0.01 µF or greater from SW to BS to power up the high-side switch.
SW	7, 8, 9, 10	Power switching output pin: This pin is the switching node that supplies power to the output and toggles between IN and GND voltage. Connect an LC filter between SW pin and the output load. Note that a capacitor is needed from SW pin to BS pin to power the high-side switch - see BS pin description.
GND	11, 12, 13	Ground pin. Heatsink and lid are connected to GND.
AGND	14	Analog ground pin, internally connected to GND. To be used according to typical application circuit only.
FB	15	Feedback input pin: The FB pin senses the divided output voltage to regulate that voltage. Drive the FB pin with a resistive voltage divider from the output voltage. The feedback threshold is 923 mV.
CMP	16	Compensation input pin: This pin is used to compensate the regulation control loop. Connect a series RC filter from CMP to AGND pin to compensate the regulation loop. In some cases, an additional capacitor is needed.

ABSOLUTE MAXIMUM RATINGS *(NOTE1)*

V_{IN} - Supply voltage ..... -0.3 V to +28 V
V_{SW} - Switch voltage ..... -1 V to V_{IN} + 0.3 V
V_{BS} - Boost voltage ..... V_{SW} - 0.3 V to V_{SW} + 6 V
All other pins ..... -0.3 V to +6 V

16-Lead Flatpack Thermal Resistance ***(NOTE2)***
θ_{JC} ..... 10 °C/W

T_L - Lead temperature (soldering, 10s) ..... +260 °C
T_{stg} - Storage temperature range ..... -65 °C to +150 °C

ESD Rating (HBM) ..... 4 kV

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
NOTE2 *When mounted on a standard JEDEC 2-layer board with bottom heatsink thermally connected.*

Recommended Operating Conditions

V_{IN} - Input voltage ..... +4.5 V to +24 V
V_{OUT} - Output voltage ..... +0.923 V to +21 V
T_A - Operating ambient temperature range ..... -55 °C to +125 °C
T_J - Operating junction temperature..... ≤ +150 °C

RADIATION HARDNESS *(NOTE3)*

LDR TID biased ..... > 40 krad (Si)
LDR TID unbiased ..... > 100 krad (Si)
SEL, SEFI and SEU immune
Free from destructive SEE (SEB, SEGR, SESB) at
LET ≤ 60 MeV·cm²/mg ..... V_{IN} ≤ 13 V
LET ≤ 85 MeV·cm²/mg ..... V_{IN} ≤ 11 V
SET-free at LET ..... ≤ 35 MeV·cm²/mg

NOTE3 *For more details please request radiation report.*

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, unless otherwise specified. Typical values at T_A = 25 °C. All voltages with respect to GND / AGND.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD}	Shutdown supply current	V_{EN} = 0 V		0.5	2.5	µA
I_{IN}	Supply current	V_{EN} = 2 V, V_{FB} = 1 V		0.7	1.0	mA
V_{FB}	Feedback voltage	4.5 V < V_{IN} < 24 V	0.9	0.923	0.946	V
V_{FBth}	Feedback over-voltage threshold	V_{FB} rising	1.0	1.1	1.2	V
A_{EA}	Error amplifier voltage gain	4.5 V < V_{IN} < 24 V		600		V / V
G_{EA}	Error amplifier transconductance	ΔI_{CMP} = 10 µA		800		µA / V
$R_{DS(ON)1}$	High-side switch ON resistance			110		mΩ
$R_{DS(ON)2}$	Low-side switch ON resistance			110		mΩ
$I_{DS(off)}$	High-side switch leakage current	V_{EN} = 0 V, V_{SW} = 0 V			10	µA
$I_{DS(lim)1}$	Upper switch current limit	Minimum duty cycle	2.9	3.5		A
$I_{DS(lim)2}$	Lower switch current limit	From drain to source		1.2		A

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN} = 12 V, unless otherwise specified. Typical values at T_A = 25 °C. All voltages with respect to GND / AGND.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
G_{CS}	COMP to current sense transconductance			3.8		A / V
f_{OSC}	Oscillation frequency	V_{FB} = 0.8 V		350		kHz
$f_{OSC(sc)}$	Short-circuit oscillation frequency	V_{FB} = 0 V		110		kHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0.8 V		90		%
t_{ONmin}	Minimum ON time	***(NOTE4)***		110		ns
$V_{EN(sd_th)}$	Enable shutdown threshold voltage	V_{EN} rising	1.1	1.4	1.7	V
$V_{EN(sd_th_hyst)}$	Enable shutdown threshold voltage hysteresis			190		mV
$V_{EN(lo_th)}$	Enable lockout threshold voltage	V_{EN} rising	2.2	2.5	2.8	V
$V_{EN(lo_th_hyst)}$	Enable lockout threshold voltage hysteresis			200		mV
$V_{IN(lo_th)}$	Input under-voltage lockout threshold voltage	V_{IN} rising	3.6	4.0	4.4	V
$V_{IN(lo_th_hyst)}$	Input under-voltage lockout threshold voltage hysteresis			200		mV
I_{SS}	Soft-start current	V_{SS} = 0 V		6		µA
t_{SS}	Soft-start period	C_{SS} = 0.1 µF		15		ms
T_{sd}	Thermal shutdown	***(NOTE4)***		160		°C

NOTE4 *Not subject to production test - verified by design/characterization*

TYPICAL PERFORMANCE

V_{IN} = 12 V, V_{OUT} = 3.3 V, L_1 = 15 µH, C_{IN} = 20 µF, C_{OUT} = 44 µF, T_A = 25 °C, unless otherwise specified.

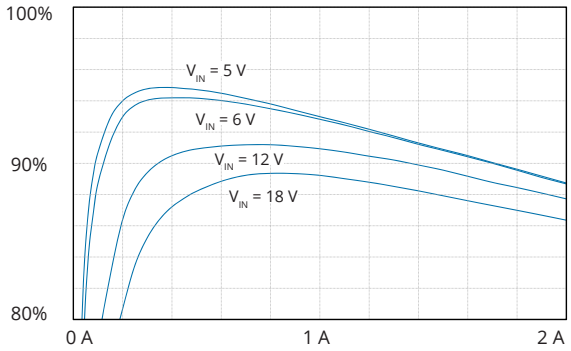


Figure 1. Efficiency over Load

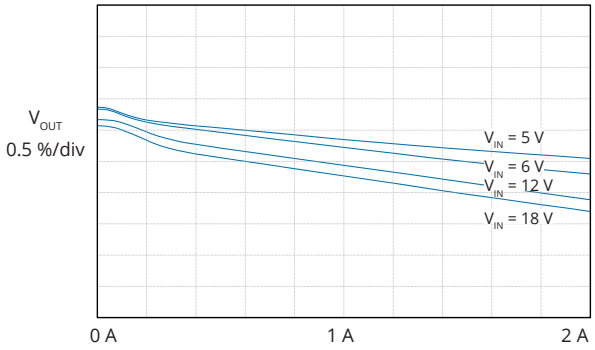


Figure 2. Line and Load Regulation

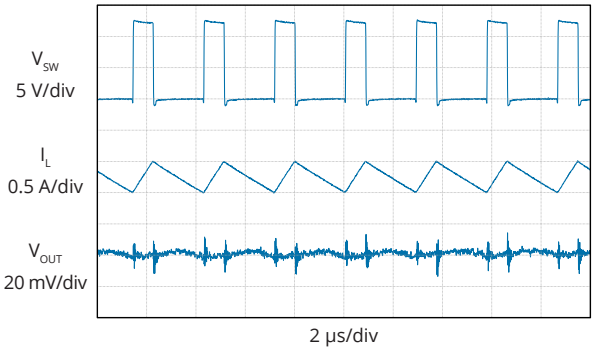


Figure 3. Steady Operation at 1 A Load

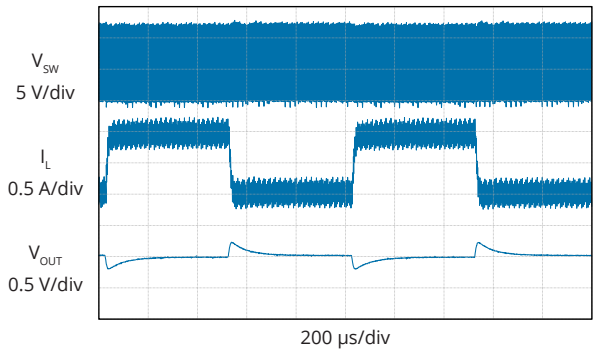


Figure 4. Load Current Toggling 1 A / 2 A

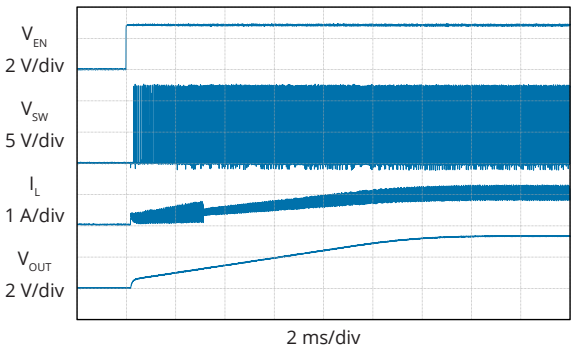


Figure 5. Startup into 1 A Load

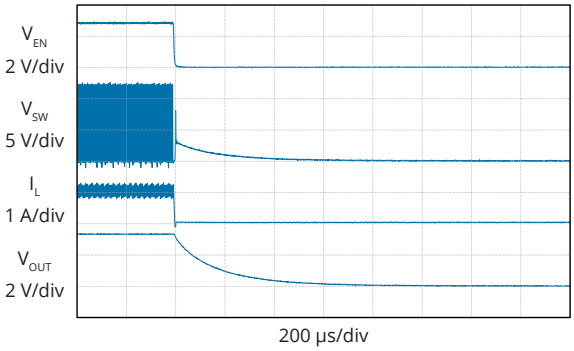


Figure 6. Shutdown at 1 A Load

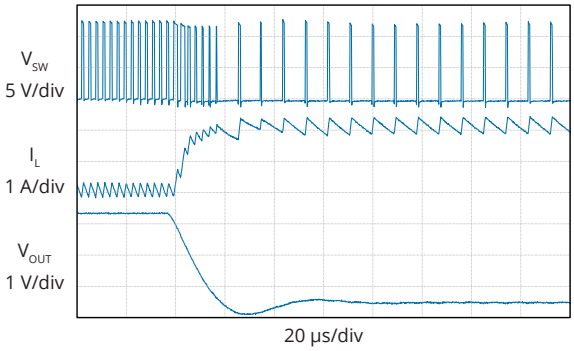


Figure 7. Entering Short Circuit from 1 A Load

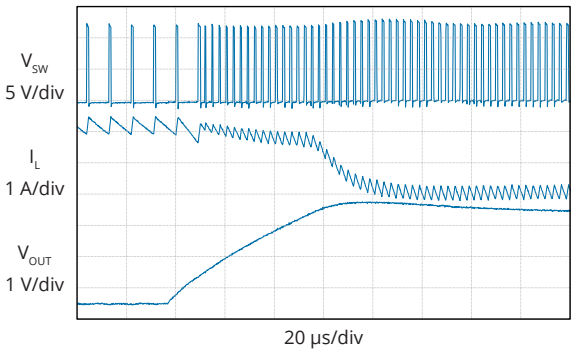


Figure 8. Short Circuit Release to 1 A Load

APPLICATION INFORMATION

The SPPL12420RH is a monolithic synchronous buck regulator featuring integrated 110 mΩ Power MOSFETs that can provide up to 2 A of load current. It regulates input voltages from 4.5 V to 24 V down to an output voltage as low as 0.923 V while providing soft-start, cycle-by-cycle over-current, under-voltage lockout and over-temperature protection.

This section of the datasheet describes typical application circuits, provides recommendations on component selection, and discusses thermal and layout design considerations.

TYPICAL APPLICATIONS

The SPPL12420RH uses a fixed frequency, current-mode step-down regulator architecture to deliver constant voltage to the load. Figure 9 shows a typical application circuit.

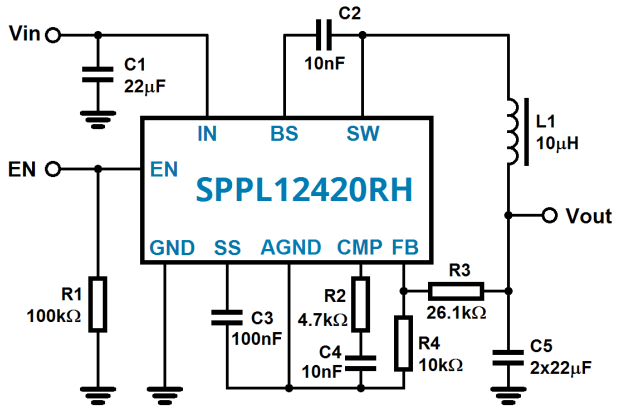


Figure 9. Typical Application Circuit

The circuit of Figure 9 takes an input voltage between 4.5 V and 24 V and regulates it down to 3.3 V while deliverging 2 A of load current.

SETTING THE OUTPUT VOLTAGE

Based on the circuit of Figure 9, the output voltage depends on the feedback voltage V_{FB} and the resistor divider network consisting of R3 and R4, as expressed with the following equation:

$$V_{OUT} = V_{FB} \cdot \frac{R_3 + R_4}{R_4}$$

The R4 resistor value may be as high as 100 kΩ, however 10 kΩ resistor value is typically recommended. Given this and the typical V_{FB} of 0.923 V, the R3 resistor may easily be calculated for a desired output voltage. Table 1 exemplifies several standard resistor values needed to achieve desired output voltage. If standard resistor values are not available a parallel combination of two standard resistors may also be used.

V_{OUT} [V]	R3 [kΩ]	R4 [kΩ]
1.0	0.0825	10
1.2	3.01	10
1.8	9.53	10
2.5	16.9	10
3.3	26.1	10
5	44.2	10

Table 1. Examples of R3/R4 for Typical Output Voltages

COMPONENT SELECTION

Inductor: The operation frequency of the SPPL12420RH allows the use of small surface mount inductors. The minimum inductance value is inversely proportional to the operating frequency and is bounded by the following limits:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{f_S \cdot I_{L(MAX)ripple} \cdot V_{IN}} [H]$$

where

- f_S = Operating frequency [Hz]
- $I_{L(MAX)ripple}$ = Allowable max inductor current ripple [A]
- V_{IN} = Input voltage [V]
- V_{OUT} = Output voltage [V]

The inductor current ripple is typically set to 20% to 40% of the maximum load current. Given this, the operating frequency and the input and output voltages for the SPPL12420RH regulator circuit, it is easy to calculate the optimal inductor value which typically ranges between 10 and 47 µH. Note that a larger value inductor will result in less ripple current and ultimately in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and lower saturation current.
Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current is given in the following equation:

$$I_{L(peak)} = I_{LOAD} + \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{2 \cdot f_S \cdot L_1 \cdot V_{IN}} [A]$$

For high efficiency, it is recommended to select an inductor with a high frequency core material (e.g. ferrite) to minimize core losses. Low ESR (equivalent series resistance) is another preferred inductor characteristic when designing for low losses. The inductor must handle the peak inductor current at full load without saturating. Note that the peak inductor current must be below the maximum switch current limit. Chip inductors typically do not have enough core to support the peak inductor currents above 1 A and are not suitable for the SPPL12420RH applications.
Lastly, select a toroid, pot core or shielded bobbin inductor for low radiated noise.

Optional Schottky Diode: During the transition between the high-side switch and the low side switch, the body diode of the low-side switch (N-channel power MOSFET) conducts the inductor current. The forward voltage of this body diode is relatively high. Therefore, an optional Schottky diode may be paralleled between SW and GND pins. The Schottky diode which features low forward voltage and fast recovery time will result in improved peak efficiency of the buck regulator circuits. The connection of the optional Schottky diode (D1) is shown in Figure 10.

Input Capacitor: The input current to the buck regulator is discontinuous, therefore, a capacitor is required to supply AC current to the regulator while maintaining the DC input voltage.
The input capacitor of Figure 9 (C1) absorbs the input switching current, therefore, it requires adequate ripple current rating. The RMS current in the input capacitor can be estimated using the following equation:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst case condition occurs when V_{IN} is twice the value of V_{OUT}. In this case, the I_{C1} is equal to the half of the load current. As a rule of thumb, select the input capacitor with the RMS current rating greater than the half of the maximum load current.
The input capacitor reduces peak currents drawn from the input source and reduces input switching noise. The input voltage ripple caused by the input capacitor can be estimated using the following equation:

$$dV_{IN} = \frac{I_{LOAD}}{C_1 \cdot f_S} \cdot \frac{V_{OUT}}{V_{IN}} \cdot (1 - \frac{V_{OUT}}{V_{IN}})$$

The input capacitor values in the range between 10 and 47 µF are sufficient in most cases. Low ESR capacitors are recommended for a low loss operation. Ceramic capacitors with X5R or X7R dielectrics are preferred, however, tantalum and electrolytic capacitors are acceptable as well. When using electrolytic or tantalum capacitors, a small (e.g. 0.1 µF), ceramic capacitors should also be used and placed as close to the IN pin as possible.

Output Capacitor: The value of the output capacitor of Figure 9 (C5) has an effect on the output voltage ripple as expressed in the following equation:

$$dV_{OUT} = \frac{V_{OUT}}{f_S \cdot L_1} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (ESR_{C5} + \frac{1}{8 \cdot f_S \cdot C_5})$$

where

- f_S = Operating frequency [Hz]
- ESR_{C5} = Equivalent series resistance of C5
- V_{IN} = Input voltage [V]
- V_{OUT} = Output voltage [V]

The output capacitor C5 can be ceramic, tantalum or electrolytic type. When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, therefore, the above equation may be simplified as the following:

$$dV_{OUT} = (1 - \frac{V_{OUT}}{V_{IN}}) \cdot \frac{V_{OUT}}{8 \cdot f_S^2 \cdot C_5 \cdot L_1}$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency, therefore, the original output voltage ripple equation can be re-written as the following expression:

$$dV_{OUT} = \frac{V_{OUT}}{f_S \cdot L_1} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot ESR_{C5}$$

To provide low output voltage ripple a minimum output capacitor value of 40 µF is recommended.

Compensation Components: The SPPL12420RH employs current mode control for easy compensation and fast transient response. System stability and transient response are controlled via CMP pin. CMP pin is the output of the internal transconductance error amplifier. A series RC network (C4 and R2 of Figure 9) sets a pole-zero combination and controls the characteristics of the control system. The DC gain of the voltage feedback loop is given by the following equation:

$$A_{VDC} = R_{LOAD} \cdot G_{CS} \cdot A_{EA} \cdot \frac{V_{FB}}{V_{OUT}}$$

where

- G_{CS} = Current sense transconductance
- A_{EA} = Error amplifier voltage gain

The system has two poles of importance. One is due to the compensation capacitor (C4 of Figure 9) and the output resistor of the error amplifier. The other one is due to output capacitor (C5 of Figure 9) and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \cdot C_4 \cdot A_{EA}}$$

$$f_{P2} = \frac{1}{2\pi \cdot C_5 \cdot R_{LOAD}}$$

where

- G_{EA} = Error amplifier transconductance

The system has one zero of importance, due to the compensation capacitor (C4) and the compensation resistor (R2). The zero is located at:

$$f_{Z1} = \frac{1}{2\pi \cdot C_4 \cdot R_2}$$

The system may also have another zero of importance due to high output capacitance and ESR of C5 (output capacitor of Figure 9). The zero is located at:

$$f_{Z2} = \frac{1}{2\pi \cdot C_5 \cdot ESR_{C5}}$$

The C6 may be added to compensate for the ESR of C5. The C6 together with R2 creates another pole which is located at:

$$f_{P3} = \frac{1}{2\pi \cdot C_6 \cdot R_2}$$

The aim of the compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system to be unstable. As a rule of thumb, the crossover frequency (f_C) below one tenth of the switching frequency is recommended. This is expressed by the following inequality:

$$f_C < \frac{f_S}{10}$$

The following steps may be used for optimizing the compensation components:

1. Select the compensation resistor, R2 to set the desired crossover frequency. The R2 resistor value can be determined using the following equation:

$$R_2 = \frac{2\pi \cdot C_5 \cdot f_C}{G_{EA} \cdot G_{CS}} \cdot \frac{V_{OUT}}{V_{FB}}$$

2. Select the compensation capacitor C4 to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, below one quarter of the crossover frequency provides sufficient phase margin. The C4 capacitor value can be determined using the following inequality:

$$C_4 > \frac{4}{2\pi \cdot R_2 \cdot f_C}$$

3. Determine if the second compensation capacitor, C6, is needed. It is needed if the ESR zero (f_{Z2}) of the output capacitor (C5) is located at less than half of the switching frequency as expressed in the following inequality:

$$\frac{f_S}{2} > \frac{1}{2\pi \cdot C_5 \cdot ESR_{C5}}$$

If the above inequality is valid, add the second compensation capacitor, C6, to set the third pole, f_{P3}, at the location of the ESR zero, f_{Z2}. The C6 capacitor value can be determined using the following equation:

$$C_6 = \frac{C_5 \cdot ESR_{C5}}{R_2}$$

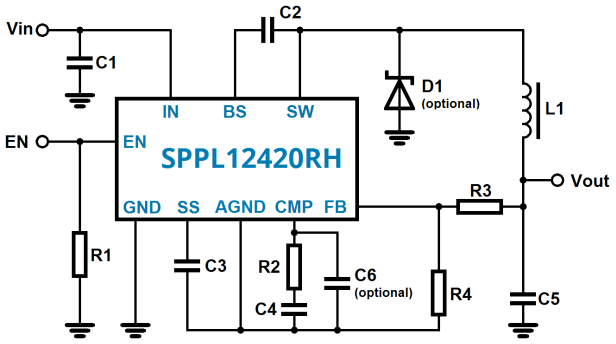
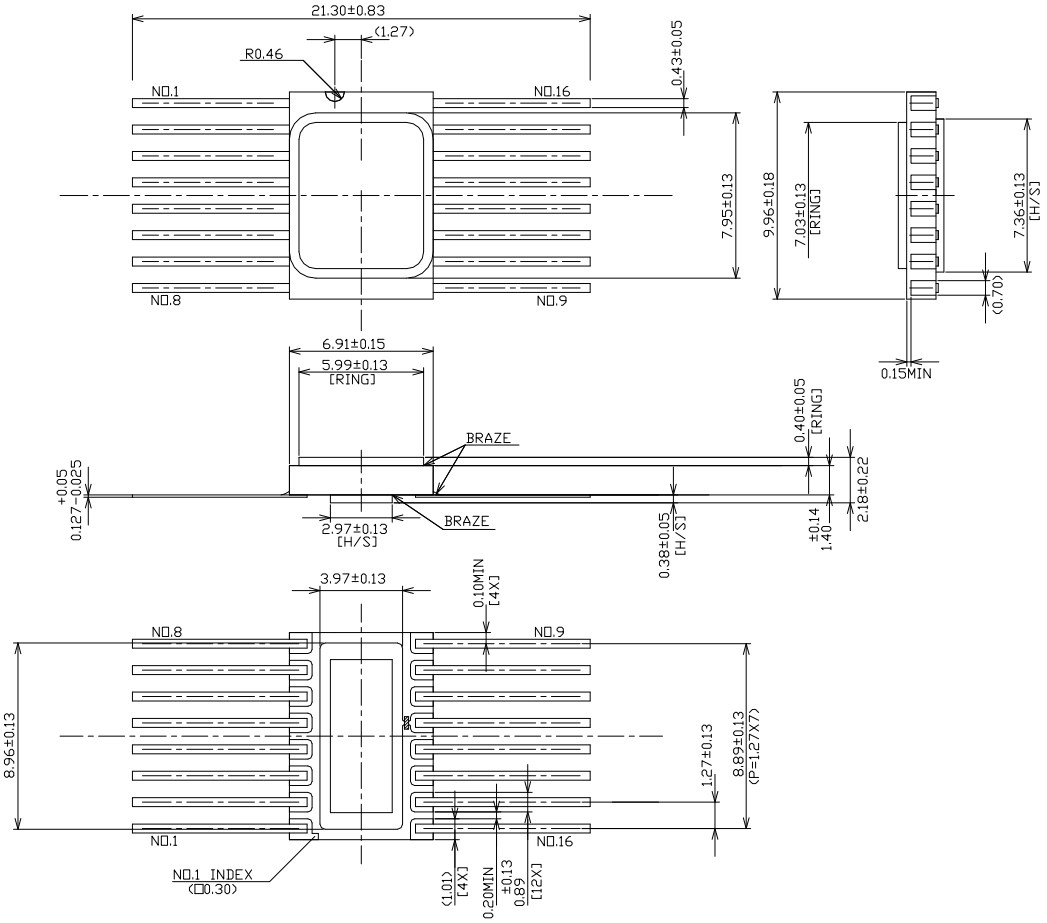


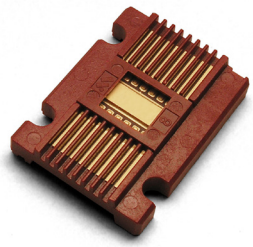
Figure 10. Application Circuit with Optional C6 and Optional D1 Schottky Diode

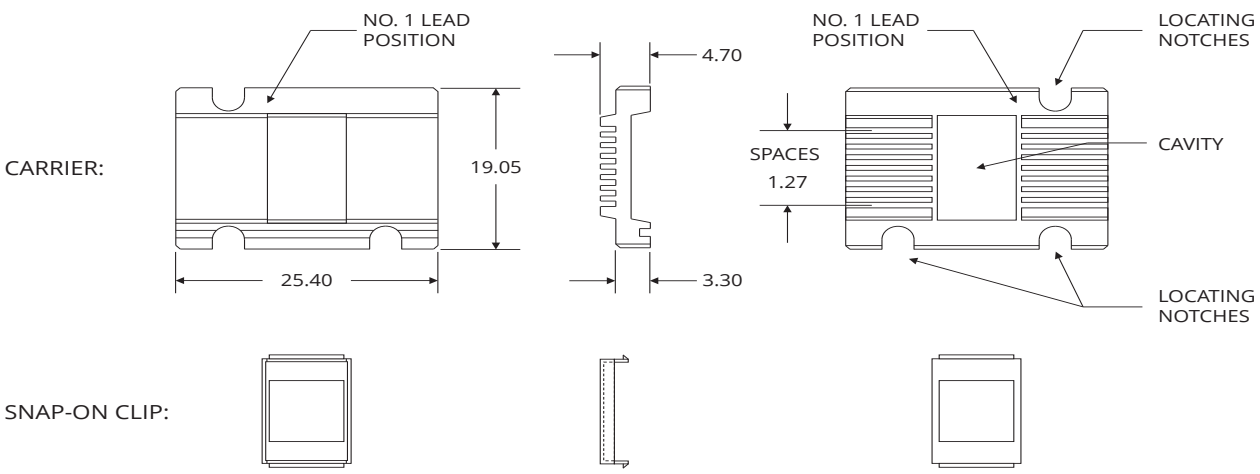
PACKAGE DIMENSION (16-LEAD FLATPACK)



PROTECTIVE CARRIER

The SPPL12420RH is delivered in a plastic carrier for mechanical protection.





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