Compact Ultra-Efficient Solar/Light Energy Harvesting Battery Charger

Benefits and Features

Ultra-low power startup:
- Cold start from 250 mV input voltage and 5 µW input power (typical).

Highly efficient energy extraction:
- Periodic open-circuit voltage sensing for Maximum Power Point Tracking (MPPT);
- Configurable MPPT ratios of 35, 50 and from 60 to 90% by 5% steps;
- Constant impedance matching (QFN package only);
- Configurable MPPT sensing timing and period;
- MPPT voltage operation range from 115 mV to 1.5 V.

Flexible energy storage management:
- Selectable overdischarge protection from 2.8 V to 4.0 V;
- Selectable overcharge protection from 3.0 V to 4.8 V;
- For any type of rechargeable battery;
- Battery charge can be disabled, e.g. during transportation.

Configuration and communication:
- Static configurations available through configuration pins (depending on package) or I²C interface;
- I²C interface to set system functionalities and read system information;
- I²C mode up to Fast Mode Plus.

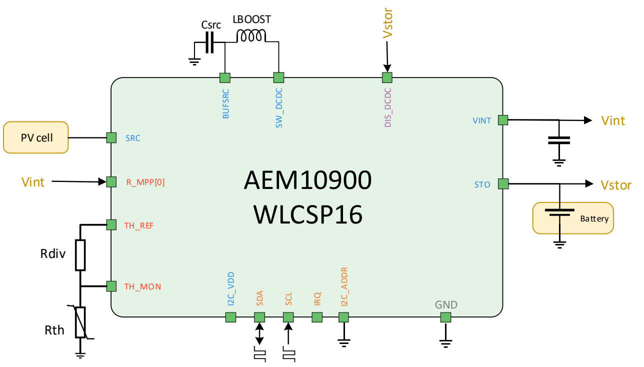
Configurable thermal protection:
- From -40°C to 125°C with accuracy below 1.5°C up to 60°C.

Power meter:
- Energy transfer or pulse counter mode.

Smallest footprint, smallest BOM:
- WLCSP16 2x2 mm or QFN28 4x4 mm;
- Only three passive components.

Applications

Wearable, Fitness	Medical Devices
Asset Tracking	IoT Sensors



Description

The AEM10900 is a fully integrated and compact battery charger circuit that extracts DC power from a solar cell to store energy in a rechargeable battery. This compact and ultra-efficient battery charger allows to extend battery lifetime and eliminates the primary energy storage in a large range of wireless application, such as wearable and medical applications, asset tracking and IoT Sensors.

Thanks to its Maximum Power Point Tracking and its ultra-low power boost converter, the AEM10900 harvests the maximum available input power from a source to charge a storage element, such as a Li-ion battery. The boost converter operates with input voltages in a range from 115 mV to 1.5 V. With its unique cold-start circuit, it can start operating with an input voltage as low as 250 mV and an input power of only 5 µW. The output voltages are in a range of 2.8 V to 4.8 V.

The configurable protection levels determine the storage element voltage protection thresholds to avoid overcharging and overdischarging the storage element and thus damaging it. Those levels are set without requiring any external component. It implements thermal monitoring for battery protection, as well as an average power monitoring system (APM) which allows the application circuit to get a measure of harvested energy.

The AEM10900 internal circuitry can be supplied either from the source or from the battery (“Keep alive” functionality). Being supplied from the battery avoids the need of a cold start after a period with no energy available on the source. On the other hand, when supplied only from the source an always positive power balance is guaranteed even if energy harvesting is not occurring for long periods of time.

It is optimal for wearable applications with its small footprint and small BOM (two capacitors and one inductor). All parameters can be set through an I²C interface, such as thermal shutoff, battery monitoring and MPPT, allowing more flexibility to customer designs.

Device Information

Package	Body size [mm]
WLCSP16	2x2
QFN28	4x4

Evaluation Board

Part number
2AAEM10900J00

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Figure 1: Simplified schematic view

1. Introduction

The AEM10900 is a full-featured energy efficient battery charger able to charge a storage element (connected to STO) from an energy source (connected to SRC).

The core of the AEM10900 is a regulated switching converter (boost) with high-power conversion efficiency.

At first start-up, as soon as a required coldstart voltage of 250 mV and a sparse amount of power of at least 5 µW is available at the source, the AEM10900 coldstarts. After the cold start, the AEM extracts the power available from the source if the input voltage is higher than 115 mV.

The AEM10900 can be fully configured through the I²C interface or partially by configuration pins (depending on the package). I²C configuration is not mandatory, as the default configuration is made to fit the most common needs, along with the configuration pins for the most common settings (depending on the package).

Through I²C communication or through the configuration pins, the user can select a specific operating mode from a variety of modes that cover most application requirements without any dedicated external component. The battery protection thresholds (Vovch and Vovdis) have a default value. They can also be configured in 60 mV steps using the I²C bus or the configuration pins STO_CFG[2:0] (QFN28 package only).

The Maximum Power Point (MPP) ratio is configurable by the configuration pins (R_MPP[2:0] on QFN28 package, R_MPP[0] on WLCSP16) or by the I²C interface. It ensures an optimum biasing of the harvester to maximize power extraction. The user can select a specific MPP ratio from two values (WLCSP16 package) or from eight values (QFN28 package), set by the configuration pins. With the I²C interface, the user can select a ratio amongst 9 different values.

Depending on the harvester, it is possible to adapt the timing between two MPP evaluations and the open circuit duration with the I²C communication but also with the configuration pins T_MPP[2:0] for the QFN28 version. There is a range of eight timing pairs.

AEM10900 features an optional temperature protection. It is set through the I²C interface and allows to define a temperature range outside which the battery will not be charged by the boost converter. One additional resistor and one additional thermistor are needed for this feature

The KEEP_ALIVE functionality sets the source to supply the AEM10900 internal circuitry VINT, which can be supplied either from the harvester connected on SRC or from the battery connected to STO. When supplied by SRC, the AEM10900 internal circuitry is running as long as enough energy is available on SRC. If no energy available on SRC, the internal voltage drops until reset voltage and the AEM need to go through a cold start before being able to charge the battery again. This is useful for applications with long periods without energy on SRC and when the I²C is not used. With this setting there is no quiescent current taken from the battery to supply the AEM10900 and the power balance is always positive. When supplied by STO, the circuit stays in SUPPLY STATE or SLEEP STATE as long as the battery connected to STO is above the over-discharge threshold. It prevents loosing the I²C configuration when energy harvesting is not occurring while minimizing the leakage on the battery.

The AEM10900 prevent the charging of the battery on STO, when the environment conditions does not allow to charge it safely thanks to the thermal monitoring.

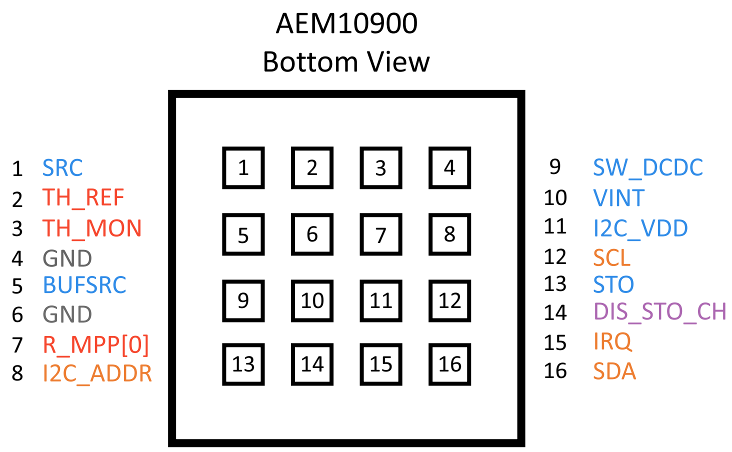


Figure 2: Pinout diagram WLCSP16

NAME	PIN NUMBER	Function
Power pins		
SRC	1	Connection to the harvested energy source.
BUFSRC	5	Connection to an external capacitor buffering the boost converter input.
SW_DCDC	9	Switching node of the boost converter.
VINT	10	Internal voltage supply.
I2C_VDD	11	Connection to I²C supply voltage. Connect to GND if not used.
STO	13	Connection to the energy storage element (battery). Cannot be left floating, voltage must always be above 2.8 V.
I²C pins		
SDA	16	Bidirectional data line. Connect to I2C_VDD if not used.
SCL	12	Unidirectional serial clock for I²C. Connect to I2C_VDD if not used.
IRQ	15	Output Interrupt request. Left floating if not used.
I2C_ADDR	8	Configuration bit for I²C address. Read as high if left floating. If set high, the address is 0x41. If set low, the address is 0x40
Configuration pins		
TH_REF	2	Reference voltage for thermal monitoring. Leave floating if not used.
TH_MON	3	Pin for temperature monitoring. Connect to VINT is not used.
R_MPP[0]	7	Used for the configuration of the MPP ratio. Read as high if left floating.
Control pins		
DIS_STO_CH	14	When asserted, the AEM stops charging the battery. Read as low if left floating.
Other pins		
GND	4, 6	Ground connection, both terminals should be strongly tied to the PCB ground plane.

Table 1: Pins description WLCSP16

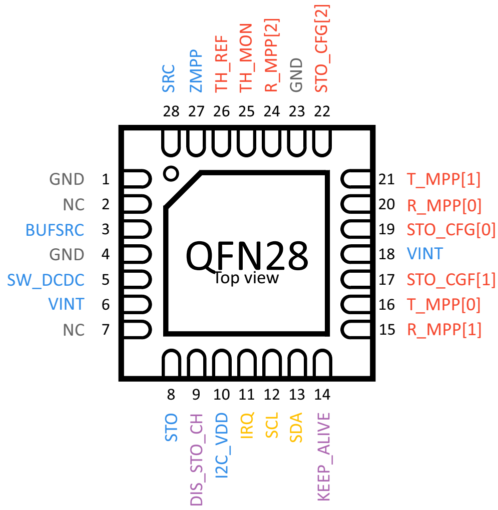


Figure 3: Pinout diagram QFN28

NAME	PIN NUMBER	Function
Power pins		
SRC	28	Connection to the harvested energy source.
BUFSRC	3	Connection to an external capacitor buffering the boost converter input.
SW_DCDC	5	Switching node of the boost converter.
VINT	6, 18	Internal voltage supply.
STO	8	Connection to the energy storage element (battery). Cannot be left floating, voltage must always be above 2.8 V.
I2C_VDD	10	Connection to supply I²C interface. Connect to GND if I²C is not used.
ZMPP	27	Connection for the ZMPP (Must be left floating when not used)
I²C pins (address 0x41)		
SDA	13	Bidirectional data line. Connect to I2C_VDD if not used.
SCL	12	Unidirectional serial clock for I²C. Connect to I2C_VDD if not used.
IRQ	11	Output Interrupt request. Leave floating if not used.
Configuration pins		
STO_CFG[0]	19	Used for the configuration of the threshold voltages for the energy storage element. Read as high if left floating.
STO_CFG[1]	17	
STO_CFG[2]	22	
T_MPP[0]	16	Used for the configuration of the MPP timings. Read as high if left floating.
T_MPP[1]	21	
R_MPP[0]	20	Used for the configuration of the MPP ratio. Read as high if left floating.
R_MPP[1]	15	
R_MPP[2]	24	
TH_REF	26	Reference voltage for thermal monitoring. Leave floating if not used.
TH_MON	25	Pin for temperature monitoring. Connect to VINT if not used.
Control pins		
DIS_STO_CH	9	When high, the AEM stops charging the battery. Read as low if left floating.
KEEP_ALIVE	14	When high, the internal circuitry is supplied from STO. When low, the internal circuitry is supplied from SRC.
Other pins		
GND	1, 4, 23,back plane	Ground connection, each terminal should be strongly tied to the PCB ground plane.
NC	2, 7	Not connected pins, leave floating.

Table 2: Pins description QFN28

2. Absolute Maximum Ratings

Parameter	Value
Voltage on STO, SRC	5.5V
Operating junction temperature	-40°C to 125°C
ESD HBM voltage	TBD
ESD CDM voltage	TBD

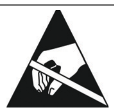
Table 3: Absolute maximum ratings

3. Thermal Resistance

Package	θJA	θJC	Unit
WLCSP16	TBD	TBD	°C/W
QFN28	TBD	TBD	°C/W

Table 4: Thermal data

ESD CAUTION



ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE
These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality

4. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$Psrc_{CS}$	Source power required for cold start	During cold start KEEP_ALIVE = Vint		5		µW
		During cold start KEEP_ALIVE = GND		14		µW
Vsrc,cs	Input voltage of the energy source to enable harvesting		0.250		1.5	V
RMPP	MPPT ratio		See Table 8			%
Vmpp	Regulation voltage on SRC when extracting power.		0.115	Voc x RMPP	1.5	V
Voc	Open-circuit voltage of the source				2.0 (TBC)	V
Timing						
Tsrc	Open-circuit duration for the MPP evaluations		See Table 9			ms
Tmppt	Time between two MPP evaluations					s
Storage element						
Vsto	Voltage on the storage element		2.81		4.78	V
Vovch	Maximum voltage accepted on the storage element before disabling its charging		3	See section 8.4	4.78	V
Vovdis	Minimum voltage accepted on the storage element before stopping to supply VINT if Keep-alive is enabled.		2.81		4.05	V
Internal supply & Quiescent Current						
Vint	Internal voltage supply			2.2V		V
IQsupply	Quiescent current on VINT in SUPPLY STATE	Vsto = 3.7 V		300		nA
IQsleep	Quiescent current on VINT in SLEEP STATE	Vsto = 3.7 V		150		nA
IQsto	Quiescent current on STO when Keep-alive functionality is disabled			1		nA
Treset,sleep	Delay before reset when no energy on SRC and Keep-alive functionality disabled, or if Keep-alive is enabled but the battery voltage dropped below Vovdis	CINT = 3.3 µF (leakage neglected), AEM in SLEEP STATE, no I²C communication		2.2		s
Treset,supply		CINT = 3.3 µF (leakage neglected), AEM in SUPPLY STATE, no I²C communication		1.1		s

Table 5: Electrical characteristics

5. Recommended Operation Conditions

Symbol	Parameter		Min	Typ	Max	Unit
External Components						
LDCDC	Inductor of the boost converter		2.7	3.3	4.7	µH
CSRC	Capacitor decoupling the BUFSRC terminal		10			µF
CINT	Capacitor decoupling the internal voltage		3.3			µF
RZMPP	**Optional -** Resistor for the ZMPPT configuration (see page 25)		33		1M	Ohm
Rdiv	**Optional** - pull-up resistor for the thermal monitoring		5k	22k	33k	Ohm
Rth	**Optional** - thermistor for the thermal monitoring	R0		10k		Ohm
		Beta		3380		K
Rscl Rsda	**Optional** - pull-up resistors for the I²C interface			1k		Ohm
Logic input pins						
R_MPP[2:0]	Configuration pins for the MPP ratio	Logic high	Connect to VINT			
		Logic low	Connect to GND			
T_MPP[2:0]	Configuration pins for the MPP timings	Logic high	Connect to VINT			
		Logic low	Connect to GND			
STO_CFG[2:0]	Configuration pins for the storage element thresholds	Logic high	Connect to VINT			
		Logic low	Connect to GND			
KEEP_ALIVE	Configuration for the "Keep alive" functionality	Logic high	Connect to VINT			
		Logic low	Connect to GND			
DIS_STO_CH	Configuration for disabling the charging of the battery	Logic high	Connect to STO			
		Logic low	Connect to GND			
I²C interface pins						
VI2C_VDD	I²C interface supply pin		1.5		Vsto	V
SCL SDA	I²C interface communication pins		Pull-up to VI2C_VDD with resistors			

Table 6: Recommended operating conditions

6. Functional Block Diagram

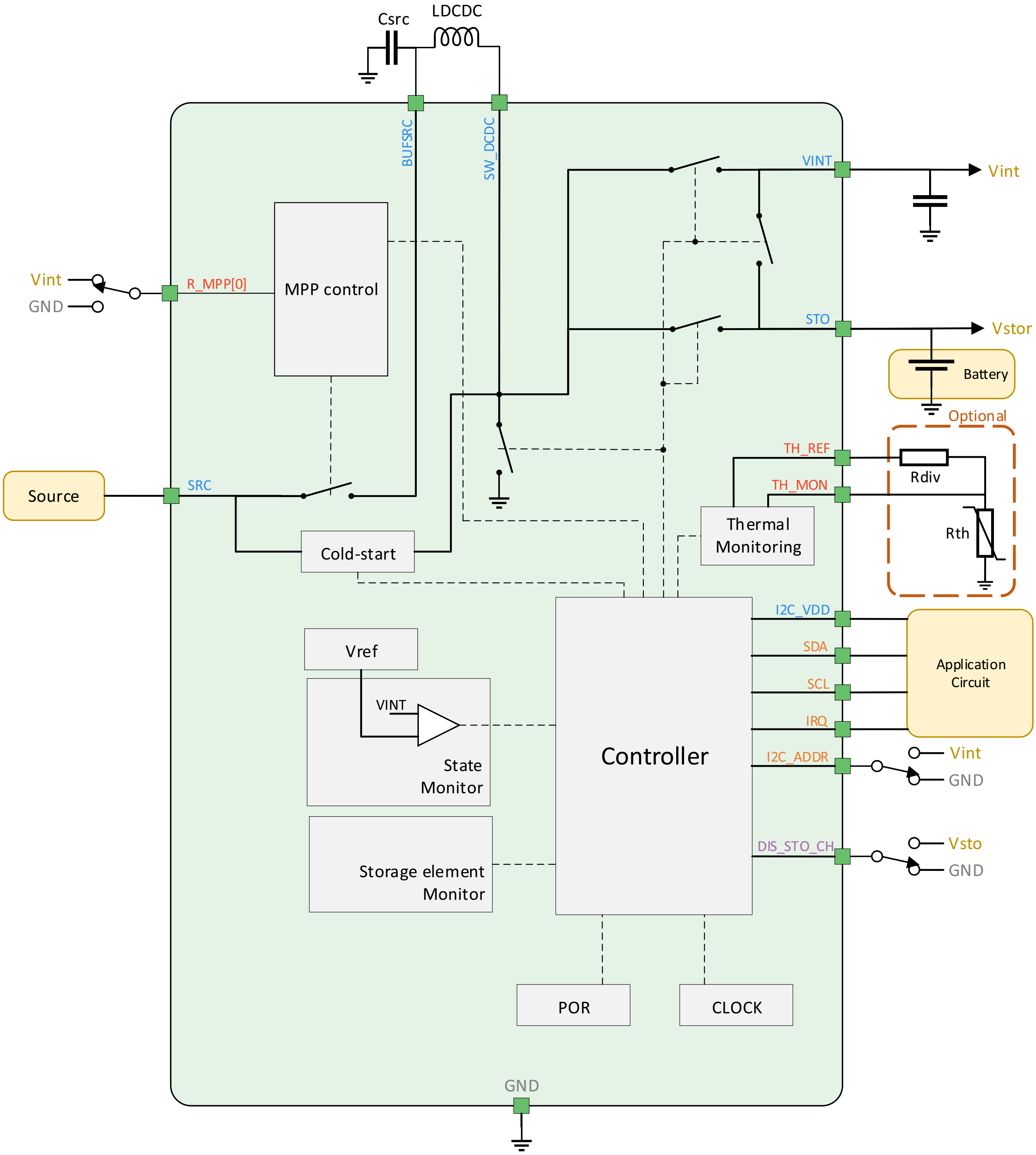


Figure 4: Functional block diagram (WLCSP16 package)

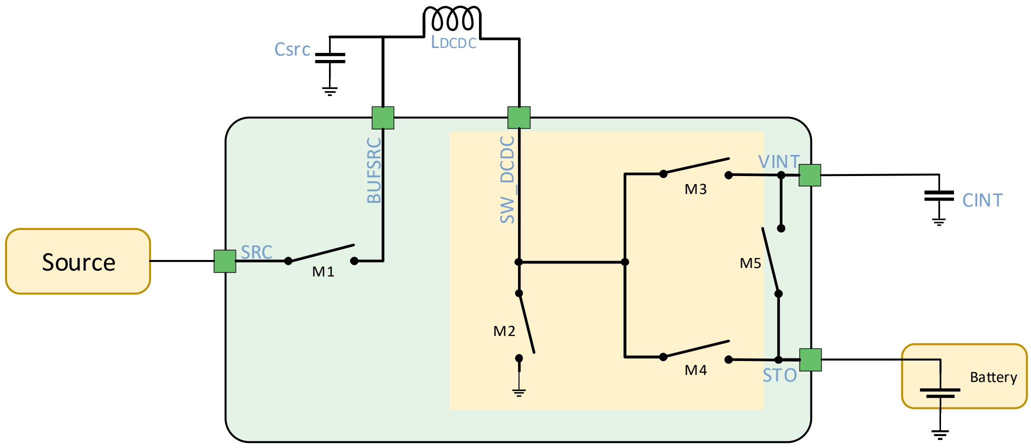


Figure 5: Simplified schematic view of the AEM10900

7. Theory of Operation

7.1. Boost Converter

The boost (step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.81 V to 4.78 V, according to the system configuration. The switching transistors of the boost converter are M2, M3 and M4. The reactive power component of this converter is the external inductor LDCDC.

Periodically, the MPP control circuit disconnects SRC and BUFSRC pins (transistor M1) in order to measure the open-circuit voltage of the harvester and evaluate the input target voltage. BUFSRC is decoupled by the capacitor CSRC, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the STO pin, which voltage is Vsto. This node is linked to the output of boost converter through transistor M4. When energy harvesting is occurring the boost converter charges the battery. M4 disconnects the storage element when Vsto reaches Vovch. If VINT drops below its regulation value and if Keep-alive functionality is disabled, the AEM switches its output by enabling M3 instead of M4 until VINT reaches its target plus a small hysteresis. If the Keep-alive functionality is enabled, VINT is instead supplied from STO by modulating the gate of M5. In this case M3 is never activated.

7.2. Maximum Power Point Tracking

During SUPPLY MODE, SENSE SRC MODE or SENSE STO MODE the voltage on SRC is regulated by an internal MPPT (Maximum Power Point Tracking) module. The MPPT module evaluates Vmpp as a constant fraction of Voc (open-circuit voltage of the source). This ratio is set by the I²C interface or with the configuration pins according to table 7. The sampling period and duration of the Voc are set according to table 8 by configuring of the T_MPP[2:0] field in the MPP register or with the configuration pins. The AEM10900 supports any Vmpp levels in the range from 115 mV to 1.5 V. It offers a choice of up to nine values for the Vmpp / Voc fraction. To maximize the power extraction from the harvester, the user must select the Vmpp / Voc ratio according to the harvester specifications.

7.3. Thermal Monitoring

Thermal monitoring allows to protect the storage element. Enabling this functionality requires the use of a resistor (Rdiv) and a thermistor (Rth). See figure 6 for external components connections. The TH_REF terminal allows a reference voltage to be applied to the resistive divider while TH_MON is the measuring point. The temperature evaluation is done periodically (typ. every 8 s) to spare power. Information for the thermal monitoring is described in section 8.7.3. Thermal monitoring is optional, if not used connect TH_MON to VINT and leave TH_REF floating.

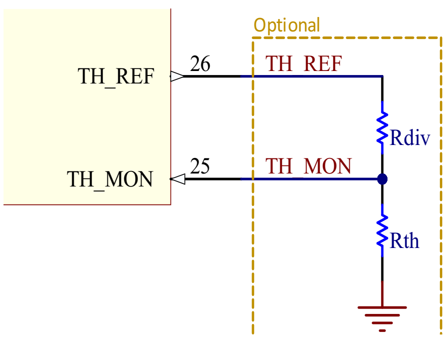


Figure 6: TH_REF and TH_MON connections

7.4. Average Power Monitoring

The Average Power Monitoring (APM) allows to evaluate the energy transfer from SRC to BAT. The APM is able to determine the transferred energy by counting the number of current pulses transferred to STO by the boost converter over a configurable time window, and thus roughly evaluate the corresponding energy.

There are two modes available. The first one allows to recover the number of current pulses and the second one the energy that is transferred by the AEM.

Refer to section 8.7.7. for further details.

7.5. Automatic High Power Mode

Automatic high-power mode allows higher currents to be extracted from SRC to STO through the boost converter. When the AEM10900 detects that the energy available on SRC is high enough, the boost converter automatically switches to high-power mode. While higher currents can be extracted from SRC in this mode, the efficiency is lower.

It might be useful to prevent switching to high-power mode for batteries sensitive to the charging current level. This feature is enabled by default and can be disabled by setting the EN_HP bit to 0 in register PWR through the I²C interface.

7.6. Keep-alive

The internal circuitry connected to VINT can be supplied either by SRC through the boost converter (Keep-alive disabled), or by the battery STO (Keep-alive enabled).

When supplied from SRC, the AEM10900 switches to RESET STATE when the energy available on SRC is not sufficient. The advantage is that no energy is pulled from the battery when the AEM10900 is not harvesting energy from SRC. The drawback is that the AEM has to cold start after every period without enough energy on SRC.

When supplied from STO, VINT is regulated as long as enough energy is available from the battery on STO, thus avoiding having to cold start if the energy on SRC is not constant.

7.7. State description

7.7.1. Reset State

In RESET STATE all nodes are deeply discharged and there is no available energy to be harvested. The AEM stays in this state until the source connected to SRC meets the coldstart requirements (Vsrc above 250 mV and Psrc above 5 µW). VINT then rises to 2.2 V, and the AEM switches to SENSE SRC STATE.

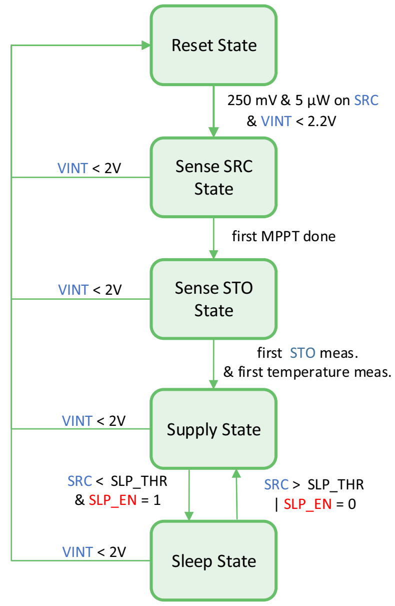


Figure 7: Diagram of the AEM10900 state

7.7.2. Sense SRC State

In SENSE SRC STATE, the AEM10900 reads the configuration pins and does a first MPPT to evaluate the power available at SRC. The MPPT is described in section 7.2.

The next step is therefore to determine whether the battery can be charged. This mode is called SENSE STO STATE.

7.7.3. Sense STO State

In SENSE STO STATE the AEM10900 does the following measurements, then switches to SUPPLY STATE:

- Battery voltage on STO;
- Temperature through pins TH_MON and TH_REF (see section 7.3. and 8.7.3.).

7.7.4. Supply State

In SUPPLY STATE, the AEM transfers charges directly from SRC to STO while maintaining Vint.

If Vint drops and the energy available on SRC is not sufficient to make Vint rise again, there are two possible behaviors, depending on the 'Keep Alive' feature:

- If 'Keep alive' is enabled, Vint is supplied by the battery through M5, so the AEM10900 stays in SUPPLY STATE while energy is available on the battery;
- If 'Keep alive' is disabled, the AEM internal circuitry will no longer be maintained and the AEM switches to RESET STATE.

7.7.5. Sleep State

In SLEEP STATE, the AEM power consumption is reduced, since the power on the input is presumably low (Vsrc below the threshold voltage defined by the SRC_DATA register). If the source voltage rises again or if the SLP_EN field of the SLEEP register is set to 0, the AEM10900 switches back to SUPPLY STATE. SLEEP STATE entering or exiting is triggered by the MPP acquisitions.

SLEEP STATE is enabled by default with a 105 mV threshold. It is not recommended to disable SLEEP STATE for standard uses of the AEM10900.

8. System Configuration

8.1. Configuration Pins and I²C

After a cold start, the AEM10900 reads the configuration pins. Those are then read periodically every 2 s, with the exception of the DIS_STO_CH pin that is read every 1 s. The configuration pins can be changed on-the-fly. The floating configuration pins are read as 1, excepted DIS_STO_CH which is read as 0.

To configure the AEM10900 through the I²C interface, user must write to the desired registers and validate the configuration by setting the USE_I2C bit of the CTRL register (0x08). The configuration pins are then ignored and all the configurations are set by the register values. All registers have a default value.

Please note that before sending the first I²C command after the AEM10900 is in RESET STATE, the user must make sure that the IRQ pin is high, notifying that the I²C interface is ready (see section 8.7.8.).

When using the I²C configuration, it is highly recommended to enable the Keep-alive functionality (see section 8.7.4.) in order to avoid losing the register configuration if no energy is available on SRC.

8.2. MPPT Configuration

Two parameters are necessary to configure the Maximum Point Tracking. The first parameter is the MPP tracking ratio, which is selected according to the characteristics of the input power source. This parameter is set on bits [3:0] of the MPPT_CFG (0x01) register, or by the configuration pins for the QFN28 package. On the WLCSP16 package, only R_MPP[0] is available as a configuration pin.

The second parameter allows configuring the duration of the evaluation of Voc and the time between two MPP evaluations. The configuration is set on bits [6:4] of the MPPT_CFG (0x01) register, or by the configuration pins for the QFN28 package.

Configuration	Availability Through Pins			MPPT ratio
R_MPP[3:0]	I²C Interface	Configuration pins		Vmpp/Voc
		QFN28	WLCSP16	
0000	yes	yes	no	ZMPP
0001	yes	yes	no	90%
0010	yes	yes	no	65%
0011	yes	yes	no	60%
0100	yes	yes	no	85%
0101	yes	yes	no	75%
0110	yes	yes	yes	70%
0111	yes	yes	yes	80%
1000	yes	no	no	35%
1001	yes	no	no	50%

Table 7: Configuration of MPP ratio

Configuration	Availability Through Pins			MPP Timing	
T_MPP[2:0]	I²C Interface	Configuration pins		Sampling duration [ms]	Sampling period [ms]
		QFN28	WLCSP16		
000	yes	no	no	2	64
001	yes	no	no	256	16384
010	yes	no	no	64	4096
011	yes	no	no	8	1024
100	yes	yes	no	4	256
101	yes	yes	no	2	128
110	yes	yes	no	4	512
111	yes	yes	yes	2	256

Table 8: Configuration of MPP timing

8.3. ZMPP Configuration

Instead of working at a ratio of the open-circuit voltage, the AEM10900 can regulate the input resistance of the boost converter so that it matches a constant resistance connected to the ZMPP pin (R_{ZMPP}). In this case, the AEM10900 regulates V_{src} at a voltage equal to the product of the ZMPP resistance and the current available at the SRC input.

8.4. Storage Element Thresholds Configuration

It is possible to set the voltage thresholds for which the storage element is considered to be discharged (Vovdis) and fully charged (Vovch).

Vovdis is configured on the STO_OVDIS (0x02) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$X = \frac{Val - 0.50625}{0.05625}$$

Val is the desired threshold value in Volts and X is the integer value to be written in the register. The minimum value is 2.8 V. If the register value corresponds to Vovdis < 2.8 V, the threshold voltage is forced to 2.8 V.

Vovch is configured on the STO_OVCH (0x03) register and encoded on 6 bits. The value to be written to the register is determined using the following equation:

$$Y = \frac{Val - 1.2375}{0.05625}$$

Val is the desired threshold value in Volts and X is the integer value to be written in the register. The minimum value is 3.0 V. If the register value corresponds to Vovch < 3.0 V, the threshold voltage is forced to 3.0 V.

On the QFN28 package, it is also possible to configure Vovdis and Vovch with configuration pins CFG[2:0] as shown in table 9.

Configuration	Availability Through Pins			Storage element threshold voltage	
CFG[2:0]	I²C Interface	Configuration pins		Vovch	Vovdis
		QFN28	WLCSP16		
000	yes	yes	no	4.50 V	3.30 V
001	yes	yes	no	4.00 V	2.80 V
010	yes	yes	no	3.63 V	2.80 V
011	yes	yes	no	3.90 V	2.80 V
100	yes	yes	no	3.90 V	3.50 V
101	yes	yes	no	3.90 V	3.01 V
110	yes	yes	no	4.35 V	3.01 V
111	yes	yes	yes	4.12 V	3.01 V

Table 9: Usage of CFG[2:0]

8.5. I²C Serial Interface

The AEM10900 uses I²C communication for configuration as well as to provide information about system status and measurement data. Communication requires a serial data line (SDA) and a serial clock line (SCL). A device sending data is defined as a transmitter and a device receiving data as a receiver. The device that controls the communication is called a master and the device it controls is defined as the slave.

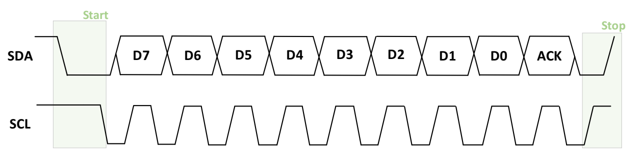


Figure 8: I²C transmission frame

The master is in charge of generating the clock, managing bus accesses and generating the start and stop bits. The AEM10900 is a slave that will receive configuration data or send the informations requested by the master.

The AEM10900 supports I²C Standard-mode (100 kHz maximum clock rate), Fast-mode (400 kHz maximum clock rate), and Fast-mode Plus (1 MHz maximum clock rate) device. Data are send with the most significant bit first.

Here are some typical I²C interface states:

- When the communication is idle, both transmission lines are pulled-up (SDA and SCL are open drain outputs);
- Start bit (S): to initiates the transmission, the master switches the SDA line low while keeping SCL high. This is called the start bit;
- Stop bit (P): to end the transmission, the master switches the SDA line from low to high while keeping SCL high. This is called a stop bit;
- Repeated Start bit (Sr): it is used as a back-to-back start and stop bit. It is similar to a start condition, but when the bus is not on idle;
- ACK: to acknowledge a transmission, the device receiving the data (master in case of a read mode transmission, slave in case of a write mode transmission) switches SDA low;
- NACK: when the device receiving data keeps SDA high after the transmission of a byte. When reading a byte, this can mean that the master is done reading bytes from the slave.

To initiate the communication, the master sends a byte with the following informations:

- Bits [7:1] is the slave address, which is 0x40 or 0x41 for the AEM10900, depending on the value of the I2C_ADDR pin. For packages where the I2C_ADDR pin is not present, the address is 0x41;
- Bit [0] is the communication mode: 0 for 'read mode' (used when the master reads informations from the slave) and 1 for 'write mode' (when the master writes informations to the slave);
- Slave replies with an ACK to acknowledge that the address has been successfully transmitted.

Here is the procedure for the master to write a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be written. For example, for the TEMP_COLD register, the master sends the value 0x04;
- Slave sends an ACK;
- Master sends the data to write to the register;
- Slave sends an ACK;
- If the master wants to write register at the next address (TEMP_HOT in our example), it sends next value to write, without having to specify the address again. This can be done several times in a row for writing several registers;
- Else the master sends a stop bit (P).

Here is the procedure for the master to read a slave register:

- Master sends the address of the slave in 'write' mode;
- Slave sends an ACK;
- Master sends the address of the register to be read. For example, for the MPPT_CFG register, the master sends the value 0x01;
- Slave sends an ACK;
- Master sends a repeated start bit (Sr);
- Master sends the address of the slave in 'read' mode;
- Slave sends an ACK;
- Master provides the clock on SCL to allow the slave to shift the data of the read register on SDA;
- If the master wants to read register at the next address (ST_OVDIS in our example), it sends an ACK and provides the clock for the slave to shift its following 8 bits of data. This can be done several times in a row for writing several registers;
- If the master wants to end the transmission, it sends a NACK to notify the slave that the transmission is over, and then sends a stop bit (P).

Both communications are described in the figure 9. Refer to table 10 for all register addresses.

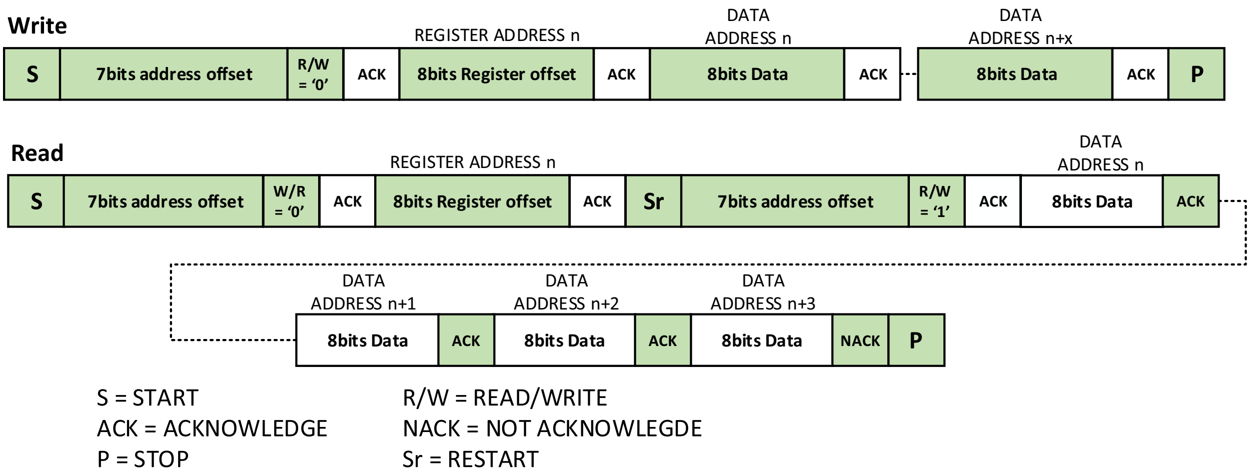


Figure 9: Read and write transmission

8.6. Registers Map

Address	Name	Bit	Field Name	Access	RESET	Description
0x00	CHIP_ID	[7:0]	CHIP_ID	R	0x00	Chip ID
0x01	MPPT_CFG	[3:0]	R_MPP	R/W	0x07 (85%)	MPPT ratio
		[6:4]	T_MPP	R/W	0x07 (2ms/256ms)	MPPT timings
0x02	STO_OVDIS	[5:0]	STO_OVDIS	R/W	0x2D (3.05V)	Overdischarge level of the storage element
0x03	STO_OVCH	[5:0]	STO_OVCH	R/W	0x33 (4.1V)	Overcharge level of the storage element
0x04	TEMP_COLD	[7:0]	TEMP_COLD	R/W	0x8F (0°C)	Cold temperature level
0x05	TEMP_HOT	[7:0]	TEMP_HOT	R/W	0x2F (45°C)	Hot temperature level
0x06	PWR	[0:0]	EN_KLIV	R/W	0x01	Keepalive enable
		[1:1]	EN _HP	R/W	0x01	High power mode enable
		[2:2]	EN_TMO	R/W	0x01	Temperature monitoring enable
		[3:3]	DIS_STO_CH	R/W	0x00	Battery charging disable
0x07	SLEEP	[0:0]	SLP_EN	R/W	0x01	Sleep mode enable
		[3:1]	SLP_THR	R/W	0x00	Sleep threshold
0x08	BAT_ADC_RATE	[2:0]	ADC_STO	R/W	0x00	ADC rate
0x09	APM	[0:0]	APM_EN	R/W	0x00	APM enable
		[1:1]	APM_MOD	R/W	0x00	APM mode
		[3:2]	APM_WIN	R/W	0x00	APM computation window
0x0A	IRQEN	[0:0]	I2C_RDY_IRQ	R/W	0x01	IRQ serial interface ready enable
		[1:1]	OVDIS_IRQ	R/W	0x00	IRQ STO OVDIS enable
		[2:2]	OVCH_IRQ	R/W	0x00	IRQ STO OVCH enable
		[3:3]	SRC_LOW_IRQ	R/W	0x00	IRQ SRC LOW enable
		[4:4]	TEMP_IRQ	R/W	0x00	IRQ temperature enable
		[5:5]	APM_IRQ	R/W	0x00	IRQ APM done enable
0x0B	CTRL	[0:0]	USE_I2C	R/W	0x00	Configuration through I²C or configuration pins
		[2:2]	SY_BUSY	R/W	0x00	Synchronization busy flag
0x0C	IRQFLG	[0:0]	I2C_RDY_F	R	0x00	IRQ serial interface ready flag
		[1:1]	OVDIS_IRQ_F	R	0x00	IRQ STOR OVDIS flag
		[2:2]	OVCH_IRQ_F	R	0x00	IRQ STOR OVCH flag
		[3:3]	SRC_LOW_IRQ_F	R	0x00	IRQ SRC LOW flag
		[4:4]	TEMP_IRQ_F	R	0x00	IRQ temperature flag
		[5:5]	APM_IRQ_F	R	0x00	IRQ APM done flag
0x0D	STATUS	[1:1]	ST_OVDIS	R	0x00	Status STO OVDIS
		[2:2]	ST_OVCH	R	0x00	Status STO OVCH
		[3:3]	ST_SRC_L	R	0x00	Status SRC LOW
		[4:4]	ST_TEMP	R	0x00	Status temperature
		[6:6]	ST_STO_CH	R	0x00	Status STO CH
0x0E	APM_DATA0	[7:0]	APM_DATA0	R	0x00	APM data 0
0x0F	APM_DATA1	[7:0]	APM_DATA1	R	0x00	APM data 1
0x10	APM_DATA2	[7:0]	APM_DATA2	R	0x00	APM data 2
0x11	TEMP_DATA	[7:0]	TEMP_DATA	R	0x00	Temperature data
0x12	STO_DATA	[7:0]	STO_DATA	R	0x00	Battery voltage
0x13	SRC_DATA	[7:0]	SRC_DATA	R	0x00	SRC ADC value

Table 10: Register summary

8.7. Registers Configurations

8.7.1. MPPT Register

The MPPT register is composed of 2 parts. The first part is reserved for the MPP ratio. This parameter is set on bits [3:0] of the register. The second part allows configuring the duration of the evaluation of Voc and the time between two MPP evaluations. The configuration is set on bits [6:4] of the register. All the information about the MPPT are available on section 7.2.

8.7.2. Storage Element Threshold Registers

The configuration of the storage element thresholds is done by setting two different registers through the I²C communication:

- The Vovdis threshold is configured in register STO_OVDIS (0x02);
- The Vovch threshold is configured in register STO_OVCH (0x03).

All the information about the storage element threshold voltage are available on section 8.4.

8.7.3. Temperature Register

The configuration of the temperature thresholds is done by setting two registers through I²C communication:

- The low temperature threshold is configured in register TEMP_COLD (0x04);
- The high temperature threshold is configured in register TEMP_HOT (0x05).

The temperature protection uses a voltage divider consisting of the resistor Rdiv and the thermistor Rth. Considering the specifications of the thermistor used, it is possible to determine the relationship between the temperature and the resistance of the thermistor. The following equation must therefore be applied to determine the value to be written to the register:

$$\mathrm{DATA} = 256 \times \frac{\mathrm{Rth}}{\mathrm{Rth} + \mathrm{Rdiv}}$$

The equation is the same for both the high and the low thresholds. DATA is the value to be written to the register, Rth is the impedance of the thermistor at the threshold temperature and Rdiv is the resistance of the voltage divider as shown on figure 6. The AEM10900 determines if the ambient temperature is within the range previously set by measuring the voltage on pin TH_MON.

For example with a Murata NCP15XH103J03RC the default thresholds are 0°C and 45°C (see table 10), which matches the specifications of most Li-Ion batteries.

8.7.4. Power Register

The PWR (0x06) register is dedicated to the power settings of the AEM10900 and is made of 4 bits:

Bit [3]	Bit [2]	Bit [1]	Bit [0]
DIS_STO_CH	EN_TMO	EN_HP	EN_KLIV
0	1	1	1

Table 11: PWR Register

Bit [3]: Battery charging disable (DIS_STO_CH).

This register is allowed in read and write mode.

Setting this bit to 0 allows the charging of the battery. Setting this bit to 1 disables it.

Bit [2]: Temperature monitoring enable (EN_TMO).

The temperature monitoring enable bit enables the monitoring of the ambient temperature.

Setting this bit to 1 enables the temperature monitoring. Setting this bit to 0 disables it.

Bit [1]: High-power mode enable (EN_HP).

Setting this bit to 1 allows the AEM to automatically enter high-power mode if needed, allowing for more power to be harvested from SRC (see section 7.5.).

Setting this bit to 0 disables automatic high-power mode.

Bit [0]: Keep alive enable (EN_KLIV).

This field defines the energy source from which the AEM10900 supplies VINT (internal circuitry).

When EN_KLIV is set to 0, VINT is supplied by SRC through the boost converter. When EN_KLIV is set to 0, VINT is supplied by STO. Refer to section 7.6. for more informations.

8.7.5. Sleep Register

The Sleep register enables the sleep mode and sets the conditions for entering the sleep mode.

Bit [3]	Bit [2]	Bit [1]	Bit [0]
SLP_THR			SLP_EN
0	0	0	1

Table 12: SLP register

Bit [3:1]: Sleep threshold (SLP_THR)

This field sets the voltage threshold below which the AEM10900 enters SLEEP STATE. Table 13 shows the available settings.

For example, if the sleep threshold is set to 010, the AEM will go into SLEEP STATE if the source voltage drops below 0.255V at the MPP ratio (Vmpp).

Configuration	Sleep threshold
000	0.105 V
001	0.202 V
010	0.255 V
011	0.3 V
100	0.36 V
101	0.405 V
110	0.51 V
111	0.6 V

Table 13: Configuration of the sleep threshold

Bit [0]: Sleep mode enable (SLP_EN)

This field enables SLEEP STATE when set to 1. When set to 0, the AEM10900 will never switch to SLEEP STATE.

8.7.6. Acquisition of STO Register

This field configures the acquisition rate of the STO ADC. Depending on the application, the source and the storage element, the user might want to increase the frequency of the acquisitions of the battery voltage, so that the acquisition rate is significantly faster than the expected voltage variation on the battery. Increasing this frequency increases the energy consumption of the AEM10900.

Configuration	Sampling rate
000	Every 1.024 s
001	Every 512 ms
010	Every 256 ms
011	Every 128 ms
100	Every 64 ms

Table 14: Acquisition rates for STO ADC

8.7.7. APM Register

Average Power Monitoring (APM) allows for estimating the energy transferred from the source to the battery over a certain period of time.

Bit [3]	Bit [2]	Bit [1]	Bit [0]
APM_WIN		APM_MOD	APM_EN
0	0	0	0

Table 15: APM register

Bit [3:2]: APM computation window (APM_WIN)

This field is used to select the APM computation window. The energy transferred is integrated over this configurable time window.

Configuration	Computation window
00	128 ms
01	64 ms
10	32 ms

Table 16: Configuration of APM computation windows

The MPP period must be at least twice longer than the APM computation window. If the user sets a value that doesn't comply with the previous condition, the AEM10900 will automatically change it to the largest compliant value.

Bit [1]: APM mode (APM_MOD)

The APM implements two modes:

- Pulse counter mode: the AEM10900 counts the number of current pulses drawn by the boost converter. This mode is enabled by setting the APM mode bit to 0;
- Power meter mode: the number of pulses during a period is multiplied by a value to obtain the energy that has been transferred taking into account the efficiency of the AEM10900. This mode is enabled by setting the APM mode bit to 1. (this section needs to be completed on next version)

Bit [0]: APM enable (APM_EN)

This field enables the APM feature. When the APM_EN bit is set to 1, it is enabled. If APM_EN is set to 0, the feature is disabled.

8.7.8. IRQEN Register

For some applications, it is interesting to have an interruption flag triggered by specific conditions on the IRQ pin. This register enables those interrupts.

Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
APM_IRQ	TEMP_IRQ	SRC_LOW_IRQ	OVCH_IRQ	OVDIS_IRQ	I2C_RDY
0	0	0	0	0	1

Table 17: IRQEN register

Bit [5]: IRQ APM done enable (APM_IRQ)

This bit enables the generation of an interrupt when new APM data is available.

When set to 0, the interrupt is disabled. When set to 1, the interrupt is enabled.

Bit [4]: IRQ temperature enable (TEMP_IRQ)

This bit enables the generation of an interrupt when the temperature crosses the minimum or maximum temperature allowed to charge the battery (see section 8.5.).

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [3]: IRQ SRC LOW enable (SRC_ LOW_IRQ)

This bit enables the generation of an interrupt when the AEM10900 sleep mode crosses the sleep mode threshold, which is set in the SLEEP register.

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [2]: IRQ STOR OVCH enable (OVCH_IRQ)

This bit enables the generation of an interrupt when the battery voltage crosses the Vovch threshold.

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [1]: IRQ STOR OVDIS enable (OVDIS_IRQ)

This bit enables the generation of an interrupt when the storage element voltage crosses the Vovdis threshold.

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

Bit [0]: IRQ serial interface ready enable (I2C_RDY)

This bit enables the generation of an interrupt when the serial interface (I^2C) is ready to communicate. This interrupt is activated by default. After a reset and before communicating through the I^2C interface, the user must check that the IRQ pin is set high, to make sure the AEM10900 is ready to communicate.

When set to 1, the interrupt is enabled. When set to 0, the interrupt is disabled.

8.7.9. Control Register

The CTRL register is used to load the configuration done through the I^2C interface. It includes two fields.

Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
					SY_BUSY		USE_I2C
0	0	0	0	0	0	0	0

Table 18: CTRL register

Bit [2]: Synchronization busy flag (SY_BUSY)

This field indicates whether the synchronization from the I^2C registers to the system registers is ongoing or not. If the bit is set to 0 then the registers are not synchronized. If the bit is set to 1 then the registers are synchronized.

Bit [0]: Load configuration (USE_I2C)

This field is used to load all the I^2C registers to the system registers and thus controls which configuration is active between the configuration pins and I^2C. If the field is set to 0, the configuration pins will be used to configure the AEM10900. If it is set to 1, the configurations performed through I^2C communications are loaded.

8.7.10. IRQFLG Register

The IRQFLG register contains all interrupt flags, corresponding to those enabled in the IRQEN register.

Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
APM_IRQ_F	TEMP_IRQ_F	SRC_LOW_IRQ_F	OVCH_IRQ_F	OVDIS_IRQ_F	I2C_RDY_F
0	0	0	0	0	0

Table 19: IRQFLG register

Bit [5]: IRQ APM done Flag (APM_IRQ_F)

This interrupt flag is set to 1 when a new APM data is available, if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption hasn't been triggered.

Bit [4]: IRQ temperature Flag (TEMP_IRQ_F)

This interrupt flag is set to 1 when the temperature crosses the minimum or maximum temperature (selected through the TEMP_MIN and TEMP_MAX registers), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption hasn't been triggered.

Bit [3]: IRQ SRC LOW Flag (SRC_ LOW_IRQ_F)

This interrupt flag is set to 1 when the source crosses the sleep voltage (selected through the SLP register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption hasn't been triggered.

Bit [2]: IRQ STOR OVCH Flag (OVCH_IRQ_F)

This interrupt flag is set to 1 when the battery crosses the overcharge voltage (selected through the STOR_OVCH register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption hasn't been triggered.

Bit [1]: IRQ STOR OVDIS Flag (OVDIS_IRQ_F)

This interrupt flag is set to 1 when the battery crosses the overdischarge voltage (selected through the STOR_OVDIS register), if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption hasn't been triggered.

Bit [0]: IRQ serial interface ready Flag (I2C_RDY_F)

This interrupt flag is set to 1 when the I²C interface is ready to communicate, if the corresponding interrupt source has been previously enabled. If this bit is 0, this interruption hasn't been triggered.

8.7.11. STATUS Register

The STATUS register contains informations about the status of the AEM10900.

Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
	ST_STOR_CH		ST_TEMP	ST_SRC_L	ST_OVCH	ST_OVDIS	
0	0	0	0	0	0	0	0

Table 20: CTRL register

Bit [6]: Status STOR CH (ST_STOR_CH)

This status indicates whether the AEM is currently charging the battery or not. If this bit is set to 0, the storage element charging is disabled. If it is set to 1, the storage element charging is enabled.

Bit [4]: Temperature Status (ST_TEMP)

This bit is set to 1 if the ambient temperature is outside the range defined by the TEMP_COLD and TEMP_HOT registers. It is set to 0 is the temperature is within this range.

Bit [3]: Status SRC LOW (ST_SRC_L)

This status indicates whether the source voltage is higher or lower than the sleep level threshold. If the source voltage is higher than the sleep level then the field is set to 0, else the field is set to 1.

Bit [2]: Status STOR OVCH (ST_OVCH)

This status indicates whether the battery is higher or lower than the overcharge level threshold. If the battery voltage rises above Vovch then the field set to 1, else it is set to 0.

Bit [1]: Status STOR OVDIS (ST_OVDIS)

This status indicates whether the battery is higher or lower than the overdischarge level threshold. If the battery voltage goes below Vovdis then the field set to 1, else it is set to 0.

8.7.12. APM Data Register

The APM data register contains APM data. Depending on the mode of the APM configured in the APM register, the data has to be processed differently.

- If the APM is used in pulse counter mode, the data will simply be distributed to the three registers below;

Register APM_DATA0							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[7:0]							

Register APM_DATA1							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[15:8]							

Register APM_DATA2							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[23:16]							

Table 21: APM_DATAx registers in pulse counter mode

- If the APM is used in power meter mode, the data and an offset will be used in order to recover the measurement. To determine the power value in nano-Joule the data must be bit-shifted to SHIFT bits (see table 22) and multiplied by a factor α TBD. This will reduce the accuracy of the measurement.

Register APM_DATA0							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[7:0]							

Register APM_DATA1							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
DATA[15:8]							

Register APM_DATA2							
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
SHIFT[3:0]				DATA[19:16]			

Table 22: APM_DATAx registers in pulse counter mode

8.7.13. Temperature data Register

This field contains the result of the ADC acquisition for the temperature monitoring. The voltage at the terminals of the voltage divider can be derived by applying the following equation, with Vref = 1 V:

$$Vth = \frac{Vref \times DATA}{256}$$

Or, in order to make a comparison with the table in the thermistor data sheet, it is possible to find the impedance of the thermistor:

$$Rth = Rdiv \times \frac{DATA}{256 - DATA}$$

8.7.14. Battery data Register

This field contains the 8 bits result from the ADC acquisition of the battery voltage. To convert the result to Volts, the following equation is applied.

$$Vbat = \frac{4.8\ V \times DATA}{256}$$

8.7.15. SRC Data Register

This register contains data reflecting the voltage level at which the input of the AEM10900 is regulated, resulting from the MPPT evaluation. To convert this value in Volts refer to table 23.

Configuration pins						Voltage Level
SRC_DATA Value						Source Voltage
0	0	0	1	0	1	0.10 V
0	0	0	1	1	0	0.11 V
0	0	0	1	1	1	0.12 V
0	0	1	0	0	0	0.14 V
0	0	1	0	0	1	0.16 V
0	0	1	0	1	0	0.17 V
0	0	1	0	1	1	0.19 V
0	0	1	1	0	0	0.20 V
0	0	1	1	0	1	0.22 V
0	0	1	1	1	0	0.23 V
0	0	1	1	1	1	0.25 V
0	1	0	0	0	0	0.27 V
0	1	0	0	0	1	0.28 V
0	1	0	0	1	0	0.30 V
0	1	0	0	1	1	0.32 V
0	1	0	1	0	0	0.35 V
0	1	0	1	0	1	0.38 V
0	1	0	1	1	0	0.41 V
0	1	0	1	1	1	0.44 V
0	1	1	0	0	0	0.47 V
0	1	1	0	0	1	0.50 V
0	1	1	0	1	0	0.53 V
0	1	1	0	1	1	0.56 V
0	1	1	1	0	0	0.59 V

Table 23: Source regulation configuration pins

Configuration pins						Voltage Level
SRC_DATA Value						Source Voltage
0	1	1	1	0	1	0.62 V
0	1	1	1	1	0	0.65 V
0	1	1	1	1	1	0.68 V
1	0	0	0	0	0	0.71 V
1	0	0	0	0	1	0.74 V
1	0	0	0	1	0	0.77 V
1	0	0	0	1	1	0.80 V
1	0	0	1	0	0	0.83 V
1	0	0	1	0	1	0.86 V
1	0	0	1	1	0	0.89 V
1	0	0	1	1	1	0.92 V
1	0	1	0	0	0	0.95 V
1	0	1	0	0	1	0.98 V
1	0	1	0	1	0	1.02 V
1	0	1	0	1	1	1.05 V
1	0	1	1	0	0	1.08 V
1	0	1	1	0	1	1.11 V
1	0	1	1	1	0	1.14 V
1	0	1	1	1	1	1.17 V
1	1	0	0	0	0	1.20 V
1	1	0	0	0	1	1.23 V
1	1	0	0	1	0	1.26 V
1	1	0	0	1	1	1.29 V
1	1	0	1	0	0	1.32 V
1	1	0	1	0	1	1.35 V
1	1	0	1	1	0	1.38 V
1	1	0	1	1	1	1.41 V
1	1	1	0	0	0	1.44 V
1	1	1	0	0	1	1.47 V
1	1	1	0	1	0	1.50 V

Table 23: Source regulation configuration pins

8.8. External Components

Storage element

The storage element of the AEM10900 must be a rechargeable battery, whose size should be chosen so that its voltage does not fall below Vovdis even during occasional current peak from the battery. To keep the chip functionaity, minimum voltage on STO pin shall never fall below 2.8V.

The monitoring of the storage element is done periodically. It is therefore possible that the storage element may be overloaded if it is incorrectly sized.

It is advisable to buffer the battery with a capacitor if the internal resistance of the battery is high, to ensure that the current pulled from the battery by the application circuit does not ever make the battery voltage fall below 2.8 V.

If a disconnection of the battery is expected (e.g. because of a user removable connector), the PCB should include a decoupling capacitor to avoid over-voltage and under-voltage during that battery disconnection.

External inductor information

The AEM10900 operates with one standard miniature inductor. LDCDC must sustain a peak current of at least 1 A and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) strongly influence the power conversion efficiency of the DCDC converter. The recommended value is 3.3 µH.

External capacitors information

CSRC

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage variations when the buck-boost converter is active. The recommended value is 10 µF.

CINT

This capacitor acts as an energy buffer for the internal voltage supply. The recommended value is 3.3 µF.

Optional external component for thermal monitoring

The following components are required for the thermal monitoring:

- One resistor, typ. 22 kΩ ±20% (PNRC0402FR-0722KL)
- One NTC thermistor, typ. R0 = 10 kΩ ±5% and Beta = 3380 K ±3% (NCP15XH103J03RC)

Optional pull-up resistors for the I²C interface

SDA and SCL must be pulled-up by resistors (1 kΩ) if the I²C interface is used. The value must be determined according to the I²C mode used.

9. Typical Application Circuits

9.1. Example Circuit 1

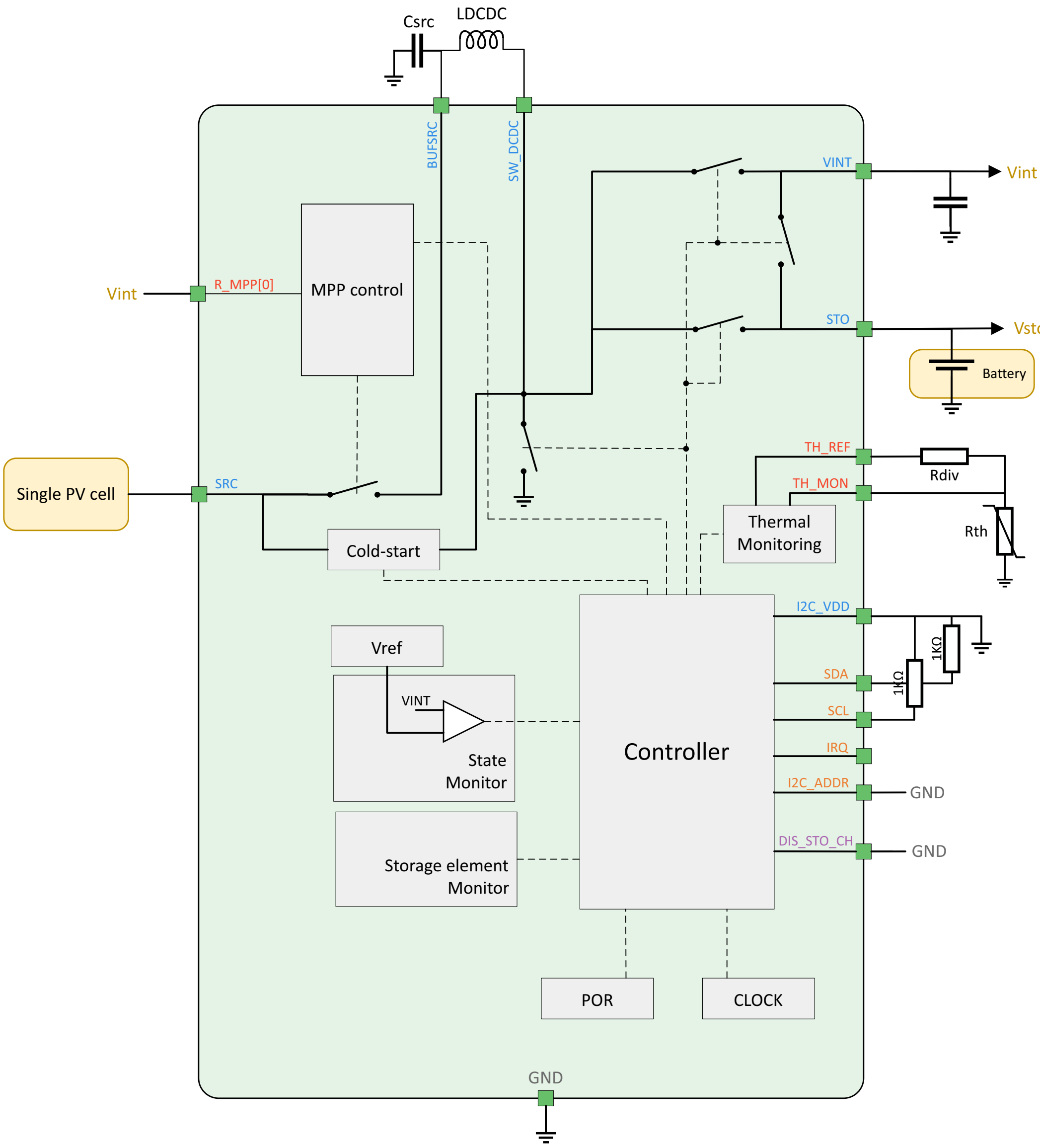


Figure 10: Typical application circuit 1

The circuit is an example of a system with solar energy harvesting with the AEM10900 (Package WLCSP16). It uses a Li-ion rechargeable battery as energy storage.

- Energy source: PV cell
- R_MPP[0] = H: The MPP ratio is set to 80%
- T_MPP: VOC timing: 2 ms; MPP evaluation period: 256 ms
- STO_CFG: The storage element is a Li-ion battery
  - Vovch = 4.12 V
  - Vovdis = 3.01 V
- The thermal monitoring is used with a default threshold value (TEMP_COLD = 0°C, TEMP_HOT = 45°C) with Rdiv = 22kOhm and Rth: NCP15XH103J03RC.
- The I²C communication is not used.
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled

9.2. Example Circuit 2

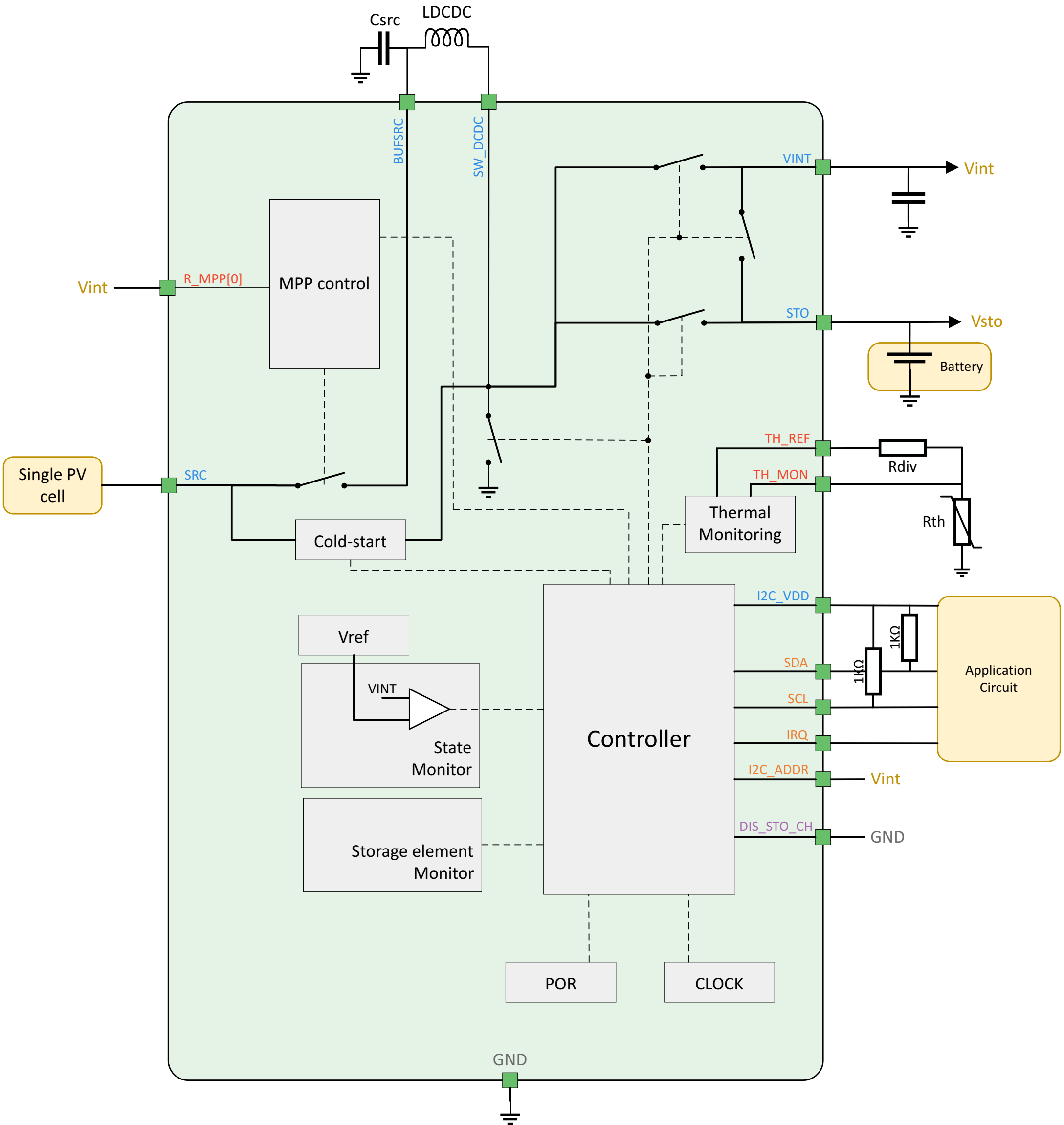


Figure 11: Typical application circuit 2

The circuit is a example of a system with solar energy harvesting with the AEM10900 (Package WLCSP16). It uses a NiCd 3 cells battery as storage element. Before to configure the registers, the AEM have the same configuration as the example circuit 1.

- Energy source: PV cell
- R_MPP: Configured through the I²C communication (MPP ratio = 90%)
- T_MPP: Configured through the I²C communication (MPP timing = 2ms/128ms)
- STO_CFG: Configured through the I²C communication
  - Vovch = 4.12 V
  - Vovdis = 3.30 V
- The thermal monitoring is used and the thresholds are configured through the I²C communication (Cold threshold = 10 °C, Hot threshold = 60 °C with Rdiv = 22kOhm and Rth: NCP15XH103J03RC.)
- DIS_STO_CH is connected to GND: The charging of the storage element on STO is enabled

Register	Value
0x01	1010001
0x02	110010
0x03	110011
0x04	01110100
0x05	00011111

Note: A configuration tool is available on the website. It helps the user to read and write on the register.

9.3. Circuit Behavior

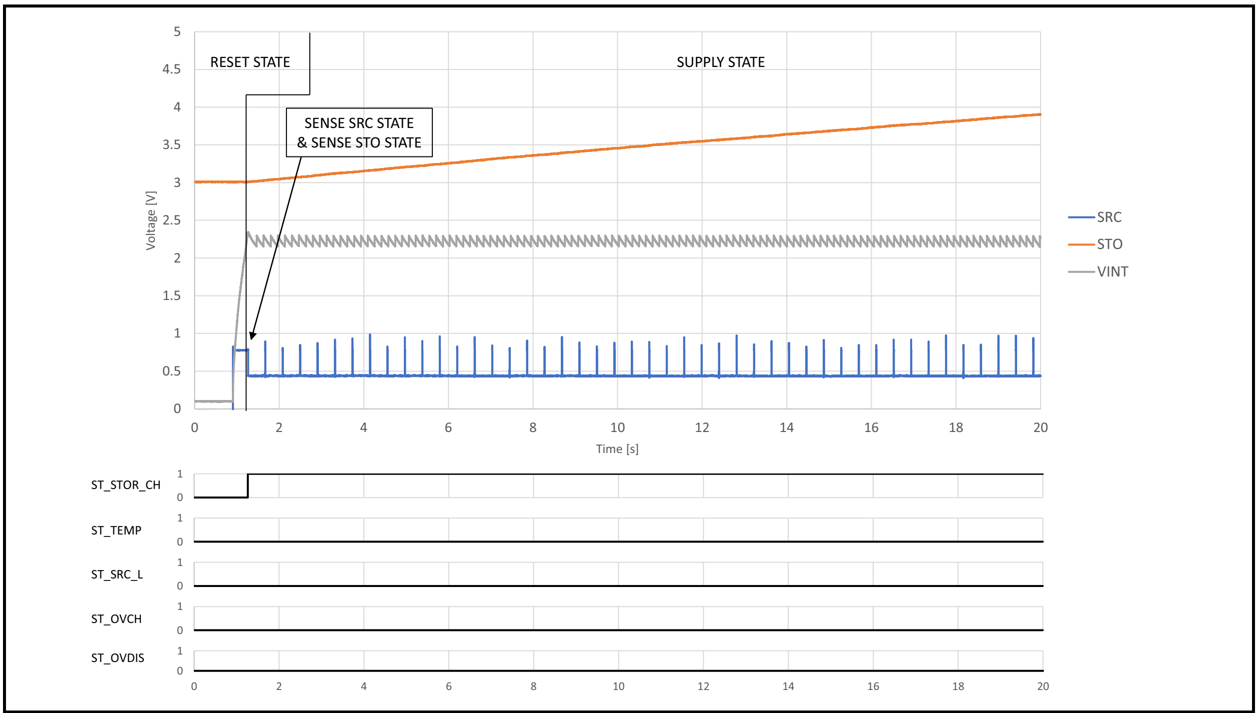


Figure 12: Start-up State

STO_CFG[3:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V), DIS_STO_CH = GND, KEEP_ALIVE = H.

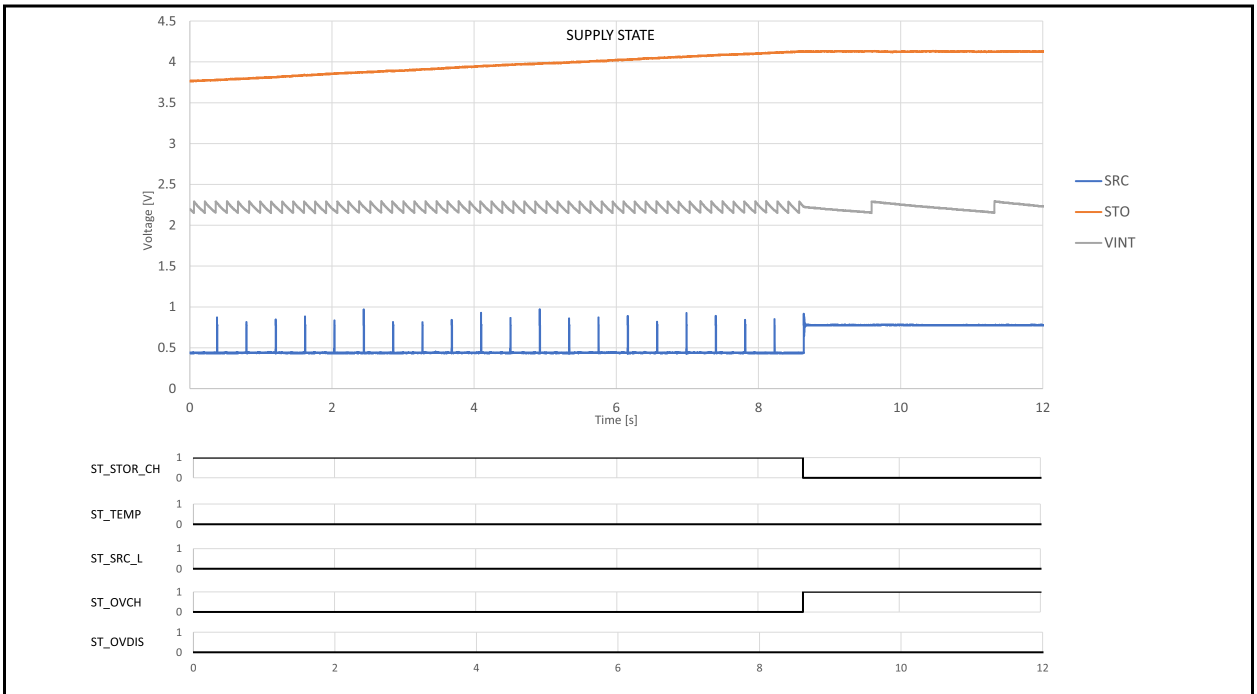


Figure 13: Supply State

STO_CFG[3:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V), DIS_STO_CH = GND, KEEP_ALIVE = H.

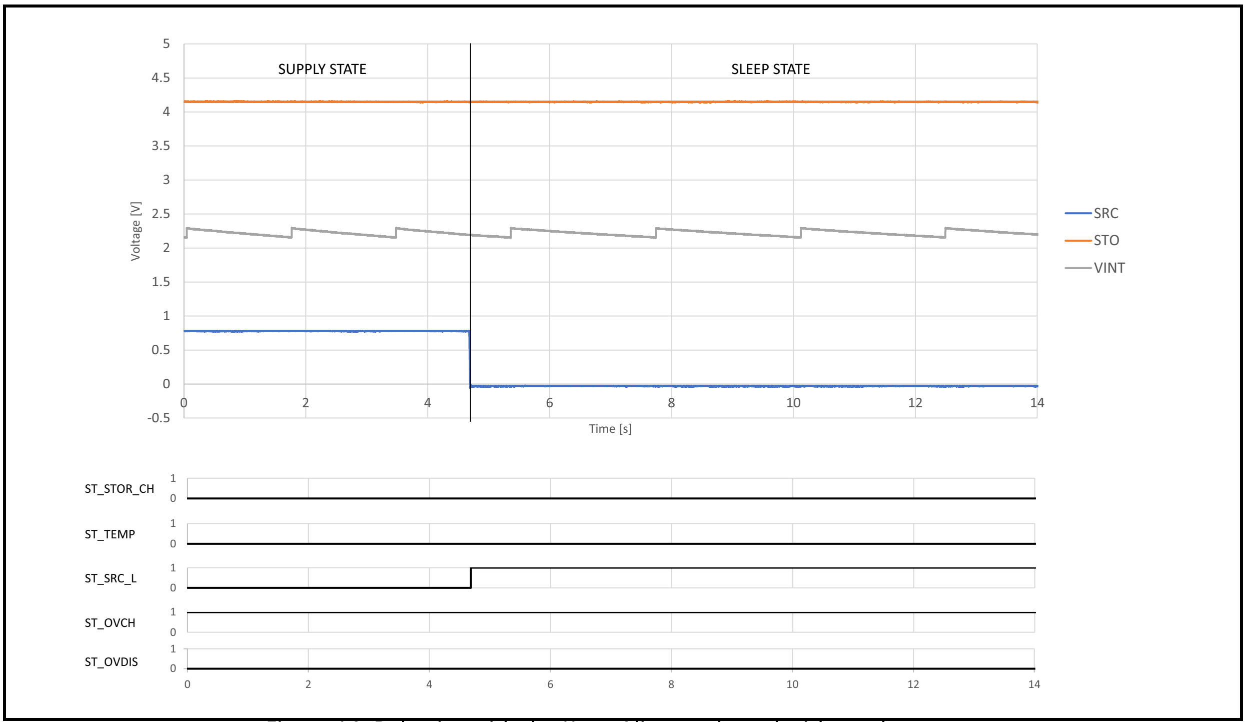


Figure 14: Behavior with the Keep Alive mode and without the source

STO_CFG[3:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V) (stop after ~4.5sec), DIS_STO_CH = GND, KEEP_ALIVE = H.

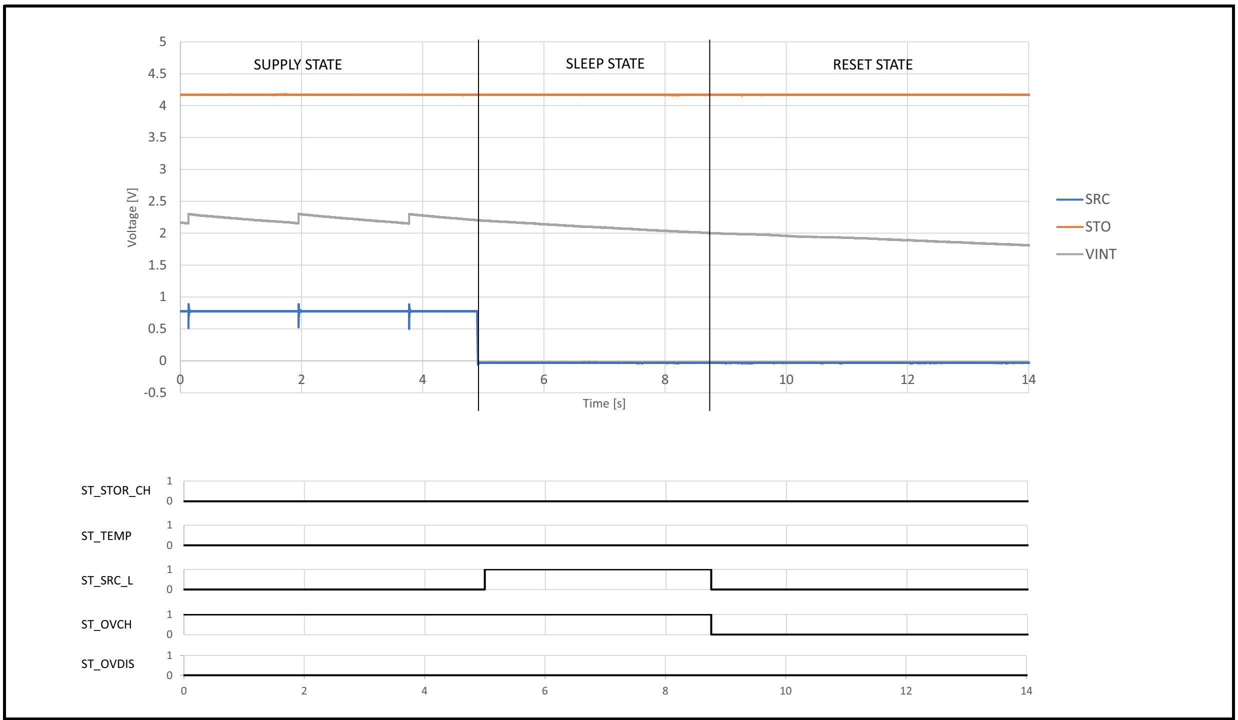


Figure 15: Behavior without the Keep Alive mode and without the source

STO_CFG[3:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 5mA with voltage compliance (0.8V) (stop after ~5sec), DIS_STO_CH = GND, KEEP_ALIVE = L.

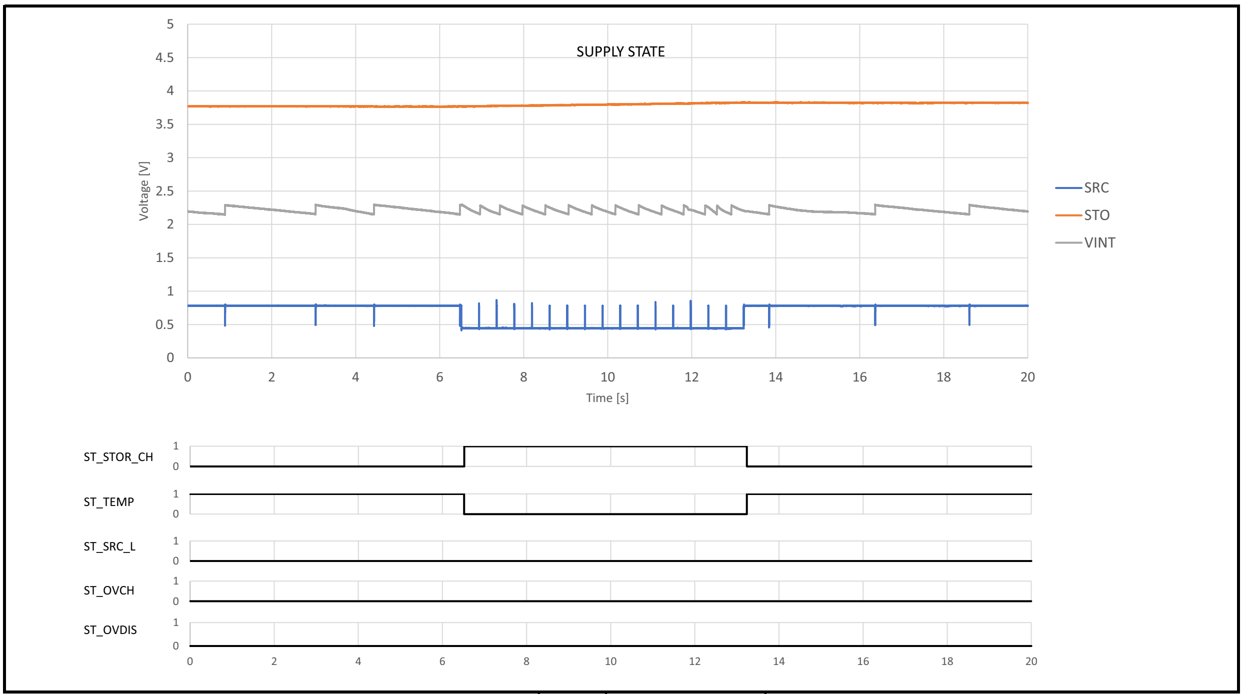


Figure 16: Thermal Monitoring Behavior

STO_CFG[3:0] = HHH, R_MPP[2:0] = LHH, T_MPP[1:0] = HL, storage element: capacitor (10mF) pre-charged to 3V, SRC: current source 1mA with voltage compliance (0.8V), DIS_STO_CH = GND, KEEP_ALIVE = H. The temperature is lower than 0°C before 6.5s and after 13.2s

10. Performance Data

10.1. DCDC Conversion Efficiency

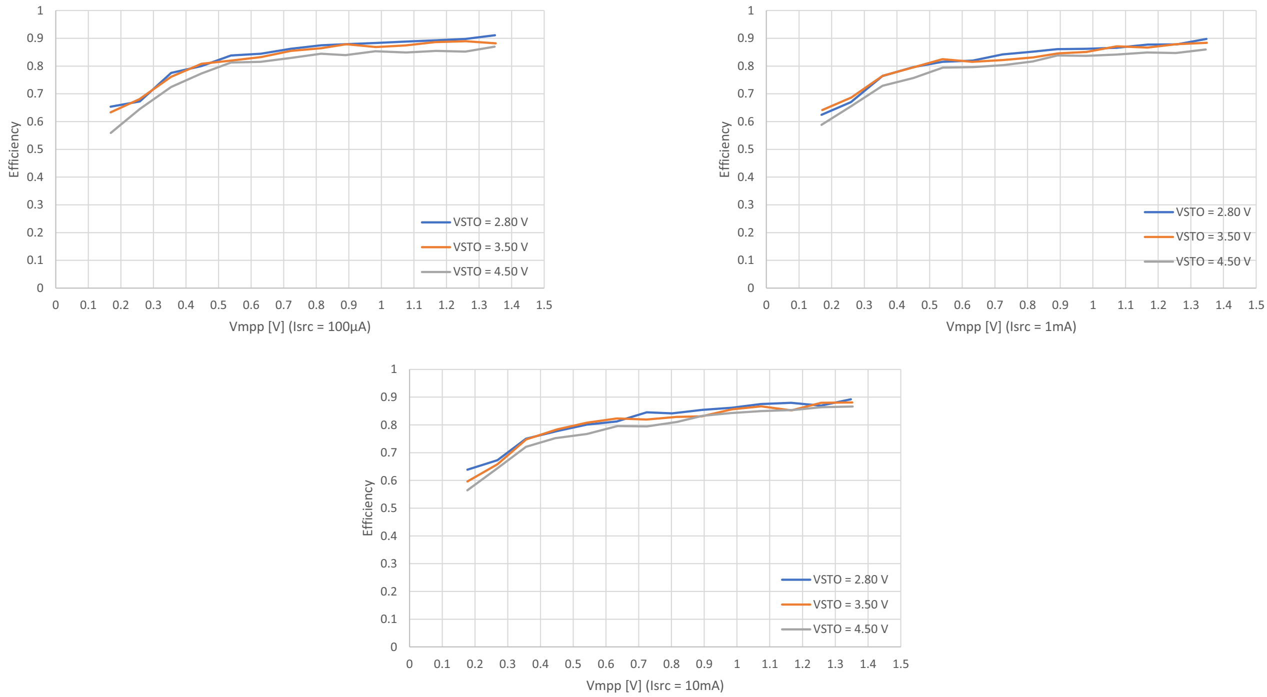


Figure 17: DCDC Conversion Efficiency (LDCDC: VLS252012HBX-4R7M-1)

10.2. Quiescent Current

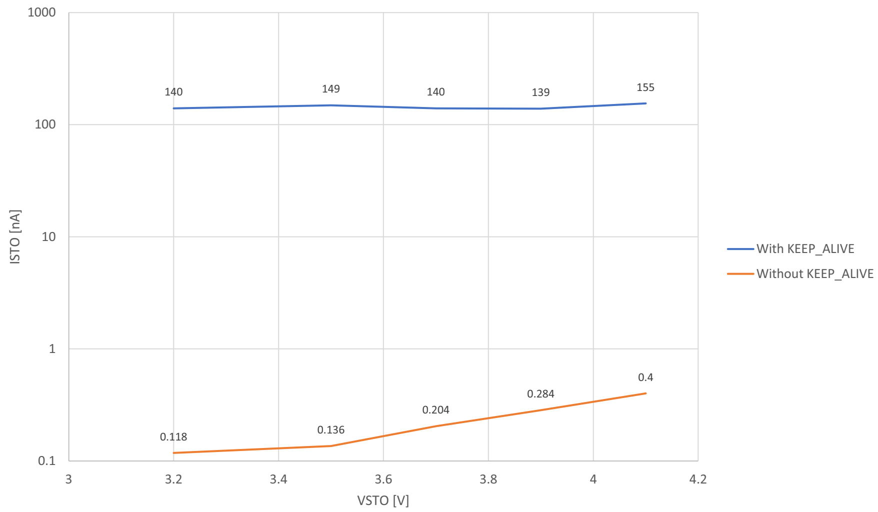


Figure 18: Quiescent Current

11. Package Information

11.1. Wafer Level Chip Scale Package (WLCSP16 2x2mm)

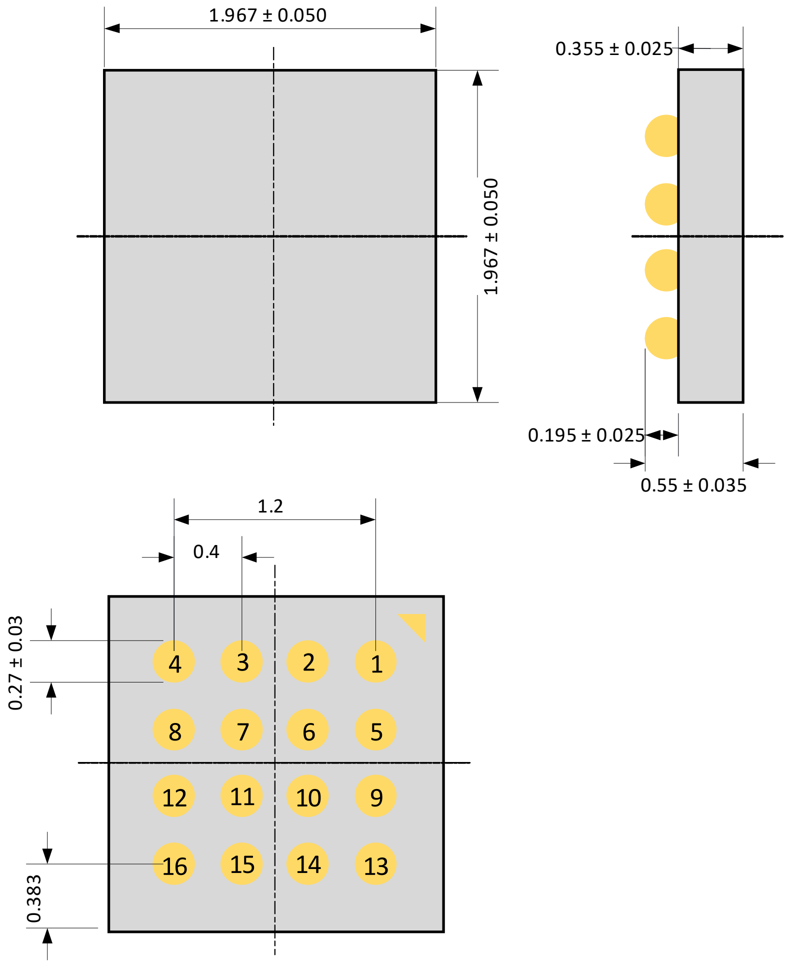


Figure 19: WLCSP16 2x2mm

11.2. WLCSP16 Board Layout

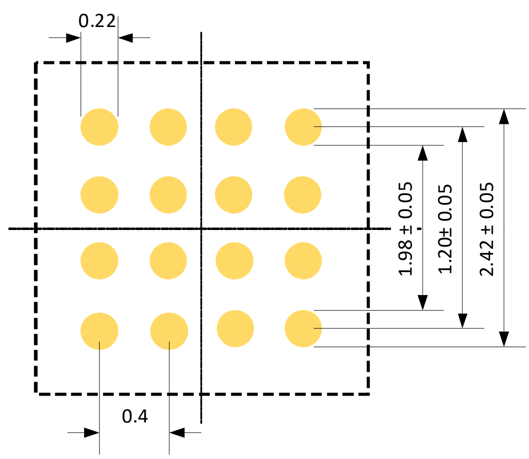


Figure 20: WLCSP16 board layer

11.3. Plastic quad flatpack no-lead (QFN28 4x4mm)

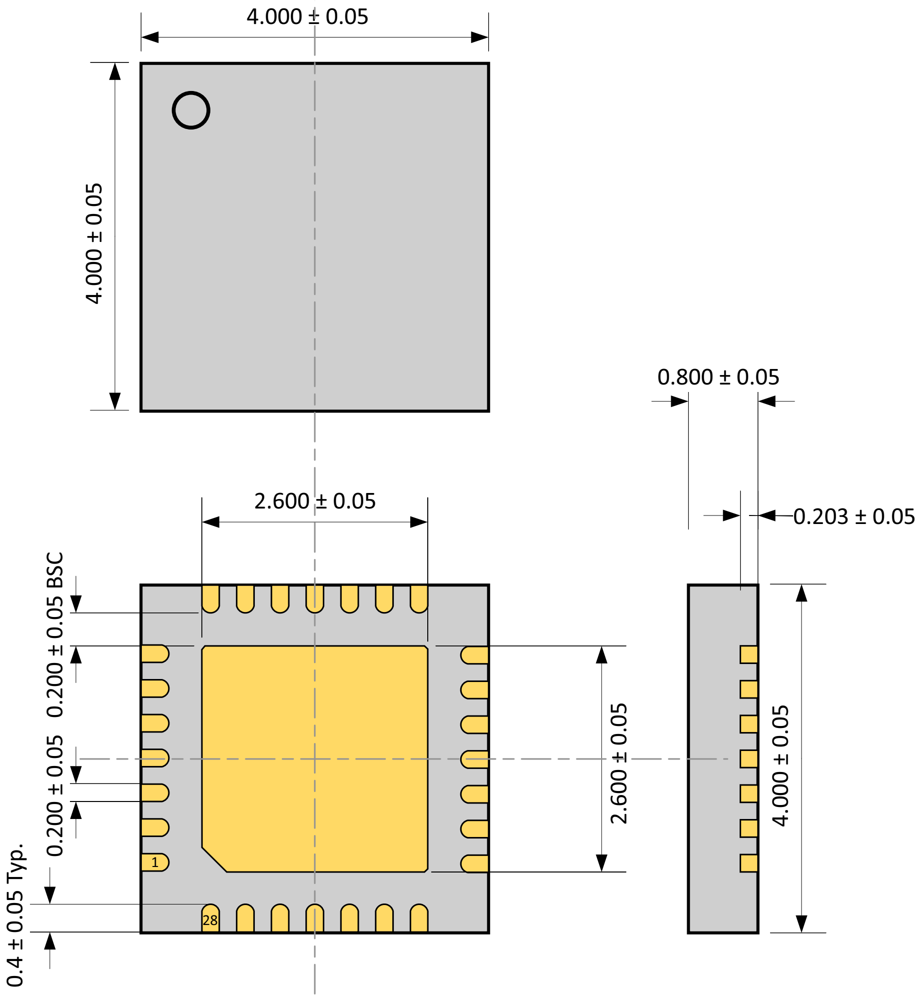


Figure 21: QFN28 4x4 mm

11.4. QFN28 Board Layout

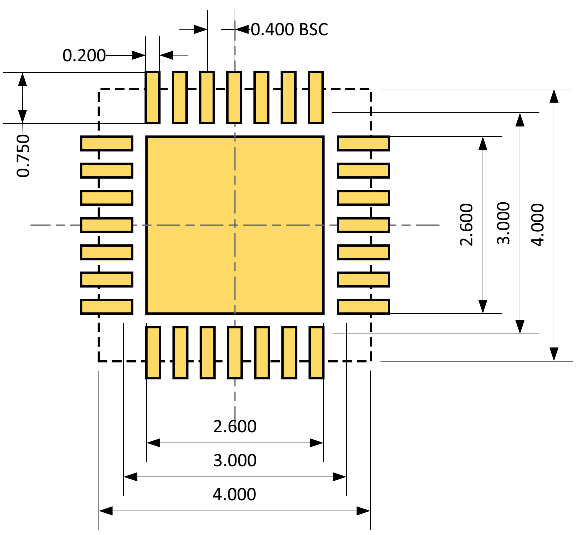


Figure 22: QFN28 4x4 mm board layout

11.5. Minimum BOM

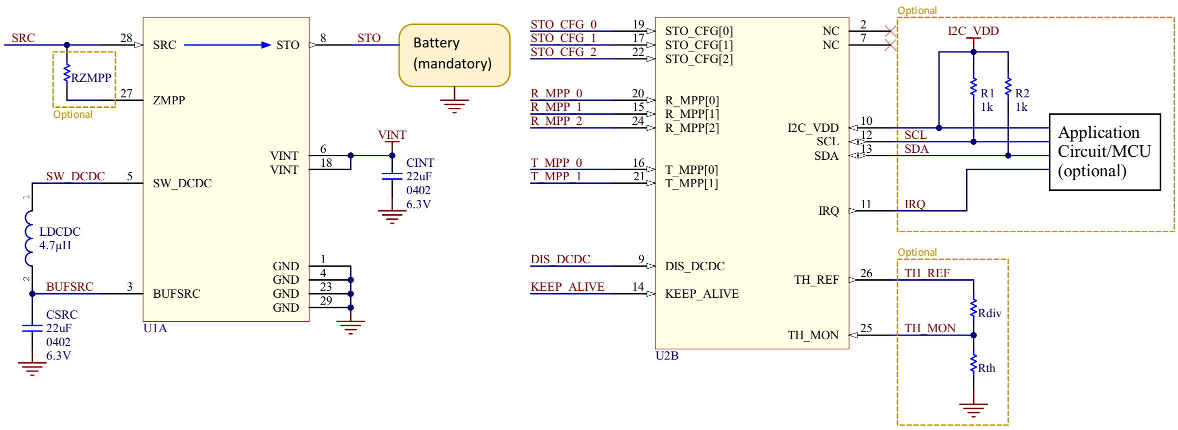


Figure 23: AEM10900 schematic

	Designator	Description	Quantity	Manufacturer	Part Number
Mandatory	U1	AEM10900	1	e-peas	order at sales@e-peas.com
	Battery	Battery with 2.8 V min. voltage	1	To be defined by user	
	LDCDC	Power inductor 4.7 µH 1.9A 1008	1	TDK	VLS252012HBX-4R7M-1
	CSRC	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
	CINT	Ceramic capacitor 22 µF 6.3 V 20% X5R 0402	1	Murata	GRM158R60J226ME01
Optional	RZMPP	Resistor for ZMPP functionality	1	To be defined by user	
	R1, R2	Pull-up 1kΩ Resistors for I²C interface	2	Yageo	AC0603FR-071KL
	Rth	10kΩ NTC thermistor for temperature monitoring	1	Murata	NCP15XH103J03RC
	Rdiv	Resistor 22kΩ 1%	1	Yageo	PNRC0402FR-0722KL

Table 24: AEM10900 bill of material

12. Revision History

Revision	Date	Description
1.0	April, 2021	Creation of the document.
1.1	April, 2021	p23 → Modification of the table 23: SRC_DATA register value Section 10. Performance: added Section 9. Typical Apllication circuits: added