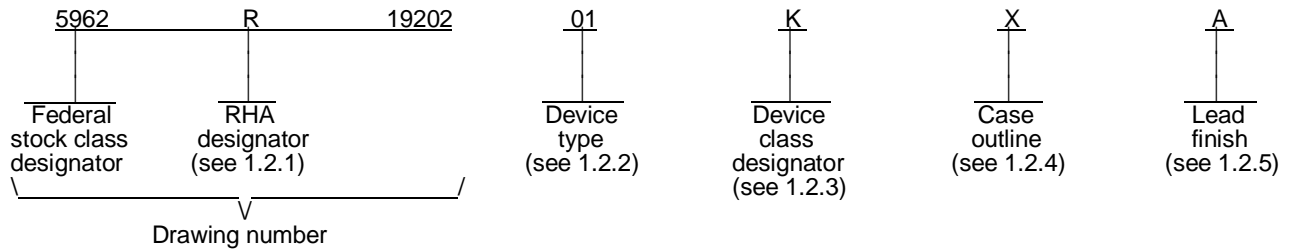


1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices meet the MIL-PRF-38534 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u> | <u>Circuit function</u> |
|--------------------|-----------------------|-------------------------------------|
| 01 | M3GB12012S | DC-DC Converter, 40 W, +12 V Output |

1.2.3 Device class designator. This device class designator is a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

| <u>Device class</u> | <u>Device performance documentation</u> |
|---------------------|---|
| K | Highest reliability class available. This level is intended for use in space applications. |
| H | Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required. |
| G | Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D). |
| E | Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance. |
| D | Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range. |

1.2.4 Case outline(s). The case outline is as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u> |
|-----------------------|-------------------------------|------------------|--|
| X | See figure 1 | 13 | Straight leads with side mounting tabs |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38534.

| | | | |
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1.3 Absolute maximum ratings. 1/ 2/

| | |
|--|-------------------|
| Input Voltage (Continuous) | 160 V dc |
| Case Operating Temperature Range (T _C) | -55°C to +125 °C |
| Lead temperature (soldering, 10 seconds)..... | +300°C |
| Storage temperature..... | -55 °C to +130 °C |

1.4 Recommended operating conditions.

| | |
|---|-----------------------|
| Input voltage range..... | +95 V dc to +140 V dc |
| Case operating temperature range (T _C)..... | -55°C to +85°C |

1.5 Radiation features. 3/

| | |
|--|---|
| Maximum total dose available (dose rate = 50 - 300 rads(Si)/s) | 100 krad(Si) 4/ 5/ |
| Neutron Irradiation (1 MeV equivalent neutrons)..... | 1x10 ¹² n/cm ² 6/ |
| Single event phenomenon (SEP) effective linear energy transfer (LET): .. | |
| No SEL, SEB, SEFI, SEGR | ≤ 82 MeV-cm ² /mg 7/ |
| SEU..... | ≤ 82 MeV-cm ² /mg 8/ |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

- MIL-PRF-19500 - Semiconductor Devices, General Specification for.
- MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.
- MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.
- MIL-STD-461 - Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment.

- 1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Device operation between +85°C and +125°C is guaranteed, but no parametric limits are specified in Table IA. For operation above the recommended maximum case temperature of +85°C contact the approved source of supply.
- 3/ See 4.3.5 for the manufacturer's radiation hardness assurance analysis and testing.
- 4/ A representative device has been High Dose Rate (HDR) tested using condition A of Method 1019 of MIL-STD-883 to 300 krad(Si) to ensure Radiation Hardness Assurance designator levels "L" of 50 krad(Si) and "R" of 100 krad(Si). A representative device will be re-tested after design or process changes that may affect the RHA response of these devices.
- 5/ The device on this SMD has not been characterized for Enhanced Low Dose Rate Sensitivity (ELDRS).
- 6/ Linear bipolar integrated circuit and bipolar semiconductor components are tested per method 1017 of MIL-STD-883 to (1x10¹² n/cm²).
- 7/ Single event performance is tested on representative devices. No Gate Ruptures, Latch-up, Burn-out, or Single Event Function Interrupts were exhibited to the limit specified. See table IB.
- 8/ Single event upsets (transient voltages) observed were within the limit specified in Table IB.

| | | | |
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DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at <https://www.astm.org/>)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table IA and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DLA Land and Maritime-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DLA Land and Maritime-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

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3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime-VA, or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) T_C as specified in accordance with table I of method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE IA. Electrical performance characteristics.

| Test | Symbol | Conditions <u>1/</u> -55°C ≤ T _C ≤ +85°C V _{IN} = +120 V dc ± 5% Full Load, C _L = 0 unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|--|---------------------|---|-------------------|-------------|-------------------|-------|-------|
| | | | | | Min | Max | |
| Output voltage | V _{OUT} | V _{IN} = 95 V dc to 140 V dc, I _{OUT} = 3.34 A | 1 | 01 | 11.95 | 12.05 | V dc |
| | | | 2,3 | | 11.88 | 12.12 | |
| | | | L, R <u>2/ 3/</u> | | 11.64 | 12.36 | |
| Output Current <u>4/</u> | I _{OUT} | V _{IN} = 95 V dc to 140 V dc <u>2/</u> | | 01 | | 3.34 | A |
| V _{OUT} Ripple Voltage | V _{RIP} | BW = 20 kHz to 10 MHz, V _{IN} = 95 V, 120 V, 140 V dc, 100 % load | 1,2,3 | 01 | | 60 | mVp-p |
| V _{OUT} Line Regulation | V _{RLINE} | V _{IN} = 95 V, 120 V, 140 V dc, 0%, 50%, 100 % load <u>2/</u> | 1,2,3 | 01 | -10 | 10 | mV dc |
| V _{OUT} Load Regulation <u>5/</u> | V _{RLOAD} | V _{IN} = 95 V, 120 V, 140 V dc, 0%, 50%, 100 % load <u>2/</u> | 1,2,3 | 01 | -60 | 60 | mV dc |
| Total Regulation | V _{Rtotal} | V _{IN} = 95 V, 120 V, 140 V dc dc, 0%, 50%, 100 % load | 1,2,3 | 01 | 11.88 | 12.12 | V dc |
| | | | | | L, R <u>2/ 3/</u> | 11.64 | |
| Input Current <u>6/</u> | I _{IN} | Pin 3 shorted to pin 2 <u>2/</u> | 1,2,3 | 01 | | 5 | mA |
| | | I _{OUT} = 0, Inhibit (pin 3) = open <u>2/</u> | | 01 | | 50 | |
| Switching Frequency | F _S | L, R <u>2/ 3/</u> | 1,2,3 | 01 | 475 | 525 | kHz |
| | | | | | 450 | 550 | |
| Sync frequency range | F _{SYNC} | Ext. Clock on Sync input (pin 4) | 1,2,3 | | 450 | 600 | kHz |
| Sync input <u>7/</u> | SYNC _{IN} | Pulse high level Pulse low level Pulse transition time Pulse duty cycle | | 01 | 4 | 10 | V |
| | | | | | -0.5 | 0.5 | V |
| | | | | | 40 | | V/μS |
| | | | | | 20 | 80 | % |
| UVR Threshold | V _{UVR} | Gradually increasing V _{IN} voltage until output enables (UVR) | 1 | 01 | 84.8 | 85.2 | V |
| | | | 2,3 | | 84.3 | 85.7 | |
| | | | L, R <u>2/ 3/</u> | | 81.2 | 93.5 | |
| UVLO Threshold | V _{UVL} | Gradually dropping V _{IN} voltage until output disables (UVL) | 1 | 01 | 81.0 | 81.8 | V |
| | | | 2,3 | | 80.6 | 82.2 | |
| | | | L, R <u>2/ 3/</u> | | 77.6 | 90.0 | |

See footnotes at end of table.

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TABLE IA. Electrical performance characteristic – Continued.

| Test | Symbol | Conditions <u>1/</u> -55°C ≤ T _C ≤ +85°C V _{IN} = +120 V dc ± 5% Full Load, C _L = 0 unless otherwise specified | Group A subgroups | Device type | Limits | | Unit |
|--|--------------------------------|---|-------------------|-------------|-------------|------------------|--------------|
| | | | | | Min | Max | |
| Enable input (inhibit function) Open circuit voltage <u>7/</u> Drive current (sink) <u>7/</u> Voltage range <u>7/</u> | | <u>8/</u> | | 01 | 3.0 -0.5 | 5.0 100 50 | V μA V |
| Efficiency <u>6/</u> | Eff | I _{OUT} = 100% load <u>2/</u> | 1,2,3 | 01 | 78 | | % |
| Isolation <u>6/</u> | ISO | 500 V dc, T _C = +25°C <u>2/</u> | 1 | 01 | 100 | | MΩ |
| Capacitive Load <u>7/ 9/</u> | C _L | No effect on DC performance, T _C = +25°C | | 01 | | 180 | μF |
| Short Circuit Power Dissipation <u>6/</u> | P _D | Short Circuit <u>2/</u> | 1,2,3 | 01 | | 18 | W |
| Overload current limit point <u>10/</u> | I _{LIM} | V _{OUT} = 90% of nominal <u>2/</u> L, R <u>2/ 3/</u> | 1 | 01 | 4.05 | 4.24 | A |
| | | | 2,3 | | 3.95 | 4.34 | |
| | | | 1,2,3 | | 3.50 | 5.00 | |
| Overload Power dissipation <u>6/</u> | P _D | V _{OUT} = 90% of nominal <u>2/</u> L, R <u>2/ 3/</u> | 1,2,3 | 01 | | 18 | W |
| | | | | | | 18.3 | |
| Line Rejection <u>7/</u> | REJ | T _C = +25°C, 100% load, dc to 50 kHz | | 01 | 40 | | dB |
| V _{OUT} Step Load Transient <u>11/</u> | V _{TLOAD} | 50% load to 100% load V _{IN} = 120 V dc | 4,5,6 | 01 | -300 | 300 | mV pk |
| V _{OUT} Step Load Transient Recovery <u>11/ 12/</u> | T _{TLOAD} | 50% Load to 100% Load V _{IN} = 120 V dc | 4,5,6 | 01 | | 200 | μs |
| V _{OUT} Step Line Transient <u>7/ 13/</u> | V _{O_TLINE} | V _{IN} = 95 V dc to/from 140 V dc | | 01 | -200 | 200 | mV pk |
| V _{OUT} Step Line Transient Recovery <u>7/ 12/ 13/</u> | T _{TLINE} | V _{IN} = 95 V dc to/from 140 V dc | | 01 | | 200 | μs |
| Turn on overshoot | V _{tonOS} | No load, full load | 4,5,6 | 01 | | 240 | mV |
| Turn on delay <u>14/</u> | T _{onD} | No load, full load L, R <u>2/ 3/</u> | 4,5,6 | 01 | 1 | 5 | ms |
| | | | | | | 6.7 | |

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

- 1/ Post irradiation testing shall be in accordance with Table II.
- 2/ A representative device has been tested using Condition A (50-300 rad(Si)/s) of Method 1019 to 300 krad(Si) for these parameters to ensure Radiation Hardness Assurance designator levels R and L. A representative device will be re-tested after design or process changes that may affect the RHA response of these devices.
- 3/ End of Life (EOL) Performance guaranteed to meet stated limits by worst-case analysis, which includes radiation, temperature, and aging effects.
- 4/ Parameter verified during line and load regulation tests.
- 5/ Percent of nominal output voltage.
- 6/ This parameter is not included in the worst-case analysis. The end-of-life tolerances are supported by post-irradiation and life test data.
- 7/ Parameter shall be tested as part of device characterization and after design and process changes. Thereafter, parameters shall be guaranteed to the limits specified in table IA.
- 8/ Enable input function is compatible with relay interface or open collector as determined in worst-case analysis.
- 9/ Capacitive load may be any value from 0 to the maximum limit without compromising DC performance.
- 10/ Current limit point is defined as the output current, relative to full rated load, such that $V_{out} = 90\%$ of the nominal output voltage.
- 11/ Load step transition time $\geq 10 \mu s$.
- 12/ Recovery time is measured from the initiation of the transient to where V_{OUT} has returned within ± 1 percent of its steady state value.
- 13/ Line step transition time $\geq 100 \mu s$.
- 14/ Turn on delay time from either a step application of input power or a logic low to a logic high transition on the inhibit pin (Pin 3) to the point where $V_{OUT} = 90\%$ of nominal.

TABLE IB. SEP test limits. 1/

| Device types | SEP | Temperature (Tc) | Conditions/Results | Effective linear energy transfer (LET) |
|--------------|----------------|------------------|--|--|
| 01 | SEU (SET) | +25°C | The largest transients are 430 mV with a duration of less than 400 μs . | $\leq 82 \text{ MeV-cm}^2/\text{mg}$ |
| 01 | SEFI Shutdowns | +25°C | None | $\leq 82 \text{ MeV-cm}^2/\text{mg}$ |
| 01 | SEL | +25°C | None | $\leq 82 \text{ MeV-cm}^2/\text{mg}$ |
| 01 | SEB | +25°C | None | $\leq 82 \text{ MeV-cm}^2/\text{mg}$ |
| 01 | SEGR | +25°C | None | $\leq 82 \text{ MeV-cm}^2/\text{mg}$ |

1/ For SEP test conditions, see 4.3.5.1.1.3 herein.

| | | | |
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Case outline X.

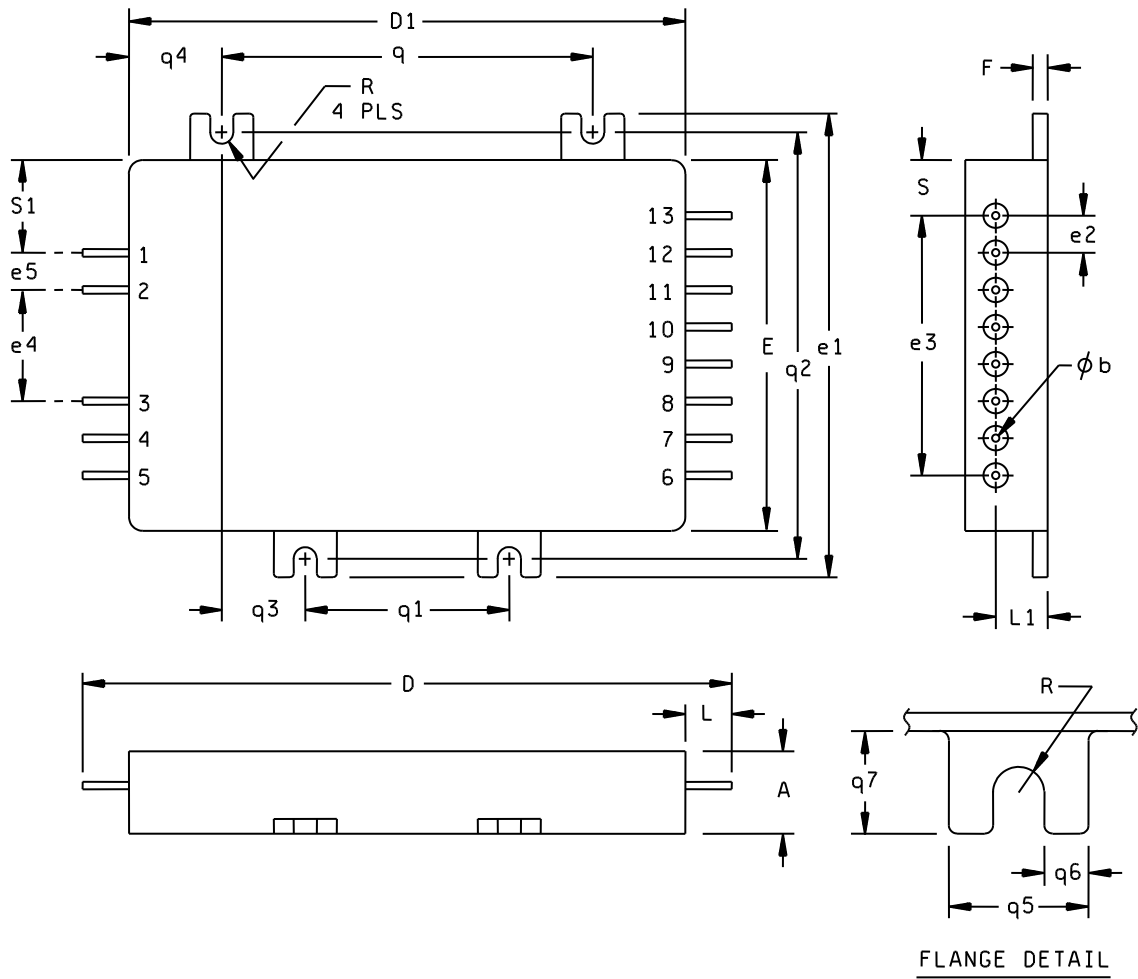


FIGURE 1. Case outline.

| | | | |
|--|------------------|----------------|-------------------|
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Case outline X - Continued.

| Symbol | Millimeters | | Inches | |
|--------|-------------|-------|-----------|-------|
| | Min | Max | Min | Max |
| A | | 12.07 | | .475 |
| D | 88.90 REF | | 3.50 REF | |
| D1 | | 77.85 | | 3.065 |
| E | | 52.20 | | 2.055 |
| e1 | 63.37 | 63.63 | 2.495 | 2.505 |
| e2/e5 | 5.05 | 5.33 | .190 | .210 |
| e3 | 35.56 REF | | 1.400 REF | |
| e4 | 14.99 | 15.49 | .590 | .610 |
| F | | 2.03 | | .080 |
| L/q7 | 6.1 | 6.6 | .24 | .26 |
| L1 | 6.48 | 6.73 | .255 | .265 |
| q | 50.55 | 55.05 | 1.99 | 2.01 |
| q1 | 27.69 | 28.19 | 1.09 | 1.11 |
| q2 | 58.17 | 58.67 | 2.29 | 2.31 |
| q3 | 11.18 | 11.68 | .44 | .46 |
| q4 | 12.57 | 12.83 | .495 | .505 |
| q5 | 9.91 | 10.41 | .39 | .41 |
| q6 | 3.30 | 3.81 | .13 | .15 |
| R | | 1.588 | | .0625 |
| S | 7.37 | 7.87 | .290 | .310 |
| S1 | 12.45 | 12.95 | .49 | .51 |
| ∅b | 0.89 | 1.14 | .035 | .045 |

NOTES:

1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Lead identification for reference only.
3. Case outline weight: 110 grams maximum.

FIGURE 1. Case outline - Continued.

| | | | |
|--|------------------|----------------|--------------------|
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| | |
|-----------------|-----------------|
| Device type | 01 |
| Case outline | X |
| Terminal number | Terminal symbol |
| 1 | +V input |
| 2 | Input return |
| 3 | Inhibit |
| 4 | Sync input |
| 5 | Sync output |
| 6 | Case ground |
| 7 | No connection |
| 8 | Output Adjust |
| 9 | - Sense |
| 10 | + Sense |
| 11 | No connection |
| 12 | Output return |
| 13 | + Output |

FIGURE 2. Terminal connections.

| | | | |
|--|------------------|----------------|--------------------|
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TABLE II. Electrical test requirements.

| MIL-PRF-38534 test requirements | Subgroups (in accordance with MIL-PRF-38534, group A test table) |
|--|---|
| Interim electrical parameters | 1, 4 |
| Final electrical parameters | 1*, 2, 3, 4, 5, 6 |
| Group A test requirements | 1, 2, 3, 4, 5, 6 |
| Group C end-point electrical parameters | 1, 2, 3, 4, 5, 6 |
| End-point electrical parameters for radiation hardness assurance (RHA) devices | 1, 2, 3, 4, 5, 6** |

* PDA applies to subgroup 1.

** Limited parameters are measured at each interim TID, and all of the subgroups listed are tested after the final exposure.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 7, 8, 9, 10, and 11 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DLA Land and Maritime-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) T_C as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5. Radiation hardness assurance (RHA). RHA qualification is required only for those devices with the RHA designator as specified herein. See table IIIA and IIIB.

| | | | |
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Table IIIA. Radiation Hardness Assurance Methods Table.

| RHA method employed | Active elements tested only as part of the hybrid device. | Tested | | Worst Case Analysis | | | | End points after final dose | |
|---------------------|---|---------------------------------------|---------------------|--|--|--|------------------------|---------------------------------------|---------------------|
| | | Element Level | Hybrid Device Level | Performed using extreme value analysis | | | | Element Level | Hybrid device level |
| | | | | Includes temperature effects | Combines temperature and radiation effects | Combines total dose and displacement effects | End-of-life | | |
| No | Tested 1X | Tested at 3X the specified TID rating | Yes | Yes | Yes | 1/ Yes | T _C = +25°C | T _C = -55°C +25°C and 85°C | |

1/ Worst case analysis performed with case temperature from -55°C to 85°C.

Table IIIB. Hybrid level and element level test table.

| Radiation Test | | Total Dose | | | Heavy Ion | Proton/Neutron |
|-----------------------------|---|---------------|------------------------------------|------------------------|-------------------------------------|--|
| | | Low Dose Rate | High Dose Rate (HDR) | ELDRS Characterization | SEP | Displacement Damage (DD) |
| Hybrid Level Testing | | Not tested | Tested (300 krad(Si)) | Not performed | Tested (82 MeV-cm ² /mg) | Not tested |
| Element Level Testing 1/ | CMOS Microcircuits | Not tested | Tested to 1.5X the level specified | Not performed | Not tested | Tested (1x10 ¹² n/cm ²) |
| | CMOS discrete (Power MOSFET) | Not tested | Tested to 1.5X the level specified | Not performed | Tested (82 MeV-cm ² /mg) | Not tested |
| | Bipolar Discrete Devices (Semiconductors) | Not tested | Tested to 1X the level specified | Not performed | Not tested | Tested (1x10 ¹² n/cm ²) |
| | Bipolar/BiCMOS Linear or Mixed Signal integrated circuit elements 2/ | Not tested | Tested to 1X the level specified | Not performed | Not tested | Tested (1x10 ¹² n/cm ²) |

1/ The device manufacturer either performs the element level testing, or purchases QML elements with documentation indicating the manufacturer has already performed the testing. See paragraphs 4.3.5.1.2.2 a and 4.3.5.2.1 a.

2/ See paragraph 4.3.5.1.2.2 b.

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4.3.5.1 Radiation Hardness Assurance (RHA) inspection. RHA qualification is required for those devices with the RHA designator as specified herein. End-point electrical parameters for radiation hardness assurance (RHA) devices shall be specified in table IA. Radiation testing will be in accordance with the qualifying activity (DLA Land and Maritime-VQ) approved plan and with MIL-PRF-38534, Appendix G.

- a. The hybrid device manufacturer shall establish procedures controlling element radiation testing, and shall establish radiation test plans used to implement element lot qualification during procurement. Test plans and test reports shall be filed and controlled in accordance with the manufacturer's configuration management system.
- b. The hybrid device manufacturer shall designate a RHA program manager to oversee element lot qualification, and to monitor design changes for continued compliance to RHA requirements.

4.3.5.1.1 Hybrid level radiation qualification.

4.3.5.1.1.1 Qualification by similarity. A family is defined by the family model designator e.g. M3GB120XXS (single output). All parts with this designator share a common design and use the same active elements with the exception of the output Schottky rectifiers. The M3GB120XXS (single output) are considered similar for the purpose of radiation testing. Device type 5962R1920201KXA (12 V single) was tested for TID and SEP and all other devices in this family maybe RHA qualified by similarity.

4.3.5.1.1.2 Total ionizing dose irradiation testing. A minimum representative device of the hybrid family (family model designator, e.g. M3GB single) is characterized and tested initially and after any design or process changes which may affect the RHA response of the device type. Devices are tested at High Dose Rate (HDR) in accordance with condition A of method 1019 of MIL-STD-883 to 300 krad(Si). The minimum sample size is two biased devices. Test results are compared to the limits specified in table IA before and after 100°C anneal for 160 hours.

4.3.5.1.1.3 Single event phenomena (SEP). Representative devices 5962-19202 (12 V) have been characterized for SEP response at initial qualification in accordance with ASTM F1192 and will be retested after any design or process changes which may affect the RHA response. Test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be normal to the die surface. No shadowing of the ion beam due to fixturing is allowed.
- b. The fluence shall be $\geq 1 \times 10^7$ particles/cm².
- c. The flux shall be between 10² and 10⁵ ions/cm²/s.
- d. The particle range shall be ≥ 50 micron in silicon.
- e. The initial characterization is performed at minimum, nominal and maximum input voltage, and with both minimum and maximum load. For future qualification the characterization will be performed only at worst case condition, maximum input voltage and maximum load. The test temperature shall be +25°C ±10 °C in air.
- f. For SEP test limits, see table IB herein.

4.3.5.1.2 Element level radiation qualification

4.3.5.1.2.1 Technologies not being tested. Testing is not performed on device technologies including: Junction Diodes, Schottky diodes, and zener diodes the manufacturer has determined to be radiation hardened.

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4.3.5.1.2.2 Total Ionizing Dose Irradiation. The manufacturer employs two methods of addressing TID.

a. RHA QML die.

1. Active Elements are purchased as level L or R (as required) per MIL-PRF-38535 Standard Microcircuit Drawing (SMD) or MIL-PRF-19500 JAN detail sheets and where the electrical performance meets those established for the elements at hybrid device design.

b. Non RHA QML die. (including QML not-RHA die or die bought to a lower RLAT level than required by the hybrid device).

1. Bipolar discrete devices - Ten biased samples from each initial wafer lot of active elements, except as noted in 4.3.5.1.2.1 will be characterized and tested at HDR in accordance with condition A of method 1019 of MIL-STD-750 to 100 krad(Si). Element parametric degradation test results are analyzed using 0.9900/90% statistics and compared to limits established for the elements at hybrid device design.
2. Bipolar/BiCMOS linear – Ten biased samples from each initial wafer lot of microcircuit elements, except as noted in 4.3.5.1.2.1, will be characterized and tested at HDR in accordance with condition A of method 1019 of MIL-STD-883, or tested using a LDR of ≤ 10 mrad(Si)/s. All MOS elements are subjected to 168 hours of accelerated anneal at 100°C. Element parametric degradation test results are analyzed using 0.9900/90% statistics and compared to limits established for the elements at hybrid device design.

4.3.5.1.3 Neutron Irradiation. All samples of CMOS, bipolar discrete, bipolar, BiCMOS, and linear or mixed signal integrated circuits described in 4.3.5.1.2.2 shall be tested to a minimum average integrated neutron fluence (1 MeV equivalent of 1×10^{12} n/cm²) in accordance with method 1017 of MIL-STD-883 or method 1017 of MIL-STD-750 prior to TID testing. 0.9900/90% statistics are applied to the element parameter degradations which are compared to limits established for the element at hybrid device design.

4.3.5.2 Radiation lot Acceptance. Each wafer lot of non-RHA QML active elements shall be evaluated for acceptance in accordance with MIL-PRF-38534 and herein except as noted in 4.5.1.2.1.

4.3.5.2.1 Total Ionizing Dose Irradiation. The manufacturer employs two methods of addressing TID.

a. QML RHA die.

1. Active Elements are purchased at the RLAT level (L or R) required by the hybrid device to a MIL-PRF-38535 (SMD) Standard Microcircuit Drawing or MIL-PRF-19500 JAN detail sheets and where the electrical performance meets those established for the element at hybrid device design.

b. Non RHA QML die.

2. Non RHA QML die (including QML not-RHA die or die bought to a lower RLAT level than required by the hybrid device) shall be tested as follows: Ten biased and two control samples from each wafer lot of active elements, except as noted in 4.3.5.1.2.1, will be characterized and tested at HDR in accordance with condition A of method 1019 of MIL-STD-883. The samples will be tested to 1X the rated value of the device (MOS components are tested to 1.5X and annealed at room temperature for 160 hours) for which it is purchased (R or L). 0.9900/90% statistics are applied to the element parametric degradations which are compared against limits established for the element at hybrid device design.

4.3.5.2.2 Neutron Irradiation. Every wafer lot of bipolar linear or mixed signal integrated circuit and semiconductor elements, except those purchased as RHA QML die will be tested to minimum average integrated neutron fluence (1 MeV Si equivalent) of 1×10^{12} n/cm² in accordance with method 1017 of MIL-STD-883 or method 1017 of MIL-STD-750 using a minimum sample size of 10 samples. 0.9900/90% statistics are applied to the element parameter degradations which are compared against limits established for the elements at hybrid device design.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Post Office Box 3990, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Occurrence of latchup (SEL).
- d. Occurrence of Burn-out (SEB).
- e. Occurrence of Gate Rupture (SEGR).
- f. Occurrence of Single Event Functional Interrupt (SEFI).
- g. Occurrence of Single Event Upset (SEU).

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-10-02

Approved sources of supply for SMD 5962-19202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DLA Land and Maritime maintains an online database of all current sources of supply <https://landandmaritimeapps.dla.mil/programs/Smcr/>.

| Standard microcircuit drawing PIN <u>1/</u> | Vendor CAGE number | Vendor similar PIN <u>2/</u> |
|---|--------------------|------------------------------|
| 5962-1920201KXA | 52467 | M3GB12012S/CKA |
| 5962-1920201KXC | 52467 | M3GB12012S/CKC |
| 5962L1920201KXA | 52467 | M3GB12012S/CKLA |
| 5962L1920201KXC | 52467 | M3GB12012S/CKLC |
| 5962R1920201KXA | 52467 | M3GB12012S/CKRA |
| 5962R1920201KXC | 52467 | M3GB12012S/CKRC |

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

52467

Vendor name and address

International Rectifier HiRel Products, Incorporated
 2520 Junction Avenue
 San Jose, CA 95134

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.