

## Features

- High efficiency and excellent thermal performance
- No minimum load requirement
- Protection against input under-voltage, output over-voltage/over-current/short circuit, and over-temperature.
- Output remote sense
- Fixed frequency operation
- 2,250Vdc input to output isolation
- Encapsulated for harsh environment
- Different temperature grades available
- Designed to meet IEC60950-1 2<sup>nd</sup> edition
- Qualification/Screening satisfy: IPC-9592, MIL-STD-810, MIL-STD-883



## Absolute Maximum Ratings

Excessive stresses over these absolute maximum ratings can cause damage to the converter. Operation should be limited to the conditions outlined under the Electrical Specifications.

Parameter	Symbol	Min	Max	Unit
Input Voltage (continuous)	$V_i$	-0.5	400	Vdc
Input Voltage (< 100ms, operating)	$V_i$	-	420	Vdc
Input Voltage (continuous, non-operating)	$V_i$	-	420	Vdc
Storage Temperature	Tstg	-55	125	°C

## Part Numbering System

FYV	EA	□□□	□	□□□	□	□	□	□	-	□
Family Name:	Input Voltage:	Output Voltage:	Enabling Logic:	Rated Output Current:	Pin Length:	Electrical Options:	Packaging	Suffix	-	Operating Temperature *Grade (°C)
FYV	EA:180-400V	Unit:0.1V 480:48V	P:positive N:negative	Unit: A 017:17A	K:0.110" N:0.145" R:0.180"	0:latch 1:latch & AUX 2:auto- restart 3:auto- restart & AUX	R: Potted, metal case	Custom code	-	H: -40 to +100 M: -55 to +100

\* Operating temperature is the temperature measured at the center of the baseplate

## Available Codes:

<b>Output Voltage</b>	5.5V	7V	12V	28V	36V	48V
<b>Output Current</b>	90A	90A	57A	28A	22A	17A

## FYVEA Series 180 – 400V Input Full Brick Converters

### Electrical Specifications

These specifications are valid over the converter's full range of input voltage, resistive load, and operating temperature unless noted otherwise.

#### Series Input Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Input Voltage	$V_i$	180	270	400	Vdc
Input Turn-on Voltage Threshold	-	172	176	180	V
Input Turn-off Voltage Threshold	-	165	170	172	V

#### Series Output Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Output Voltage Set Point Accuracy ( $V_i$ = Typical $V_{in}$ ; $I_o$ = $I_{o,max}$ ; $T_a$ = 25°C)	-	-2		+2	% $V_o$
Output Voltage Set Point Accuracy (over all conditions)	-	-3		+3	% $V_o$
Output Regulation: Line Regulation( full range input voltage, 1/2 full load)	-	-	0.2	0.5	% $V_o$
Load Regulation (full range load, Typical $V_{in}$ )	-	-	0.2	0.5	% $V_o$
Temperature ( $T_a$ = -40°C to 85 °C)	-	-	0.1	0.5	% $V_o$
Output Trim Range in % of $V_o$ ,typical	-	80	-	110	%

#### Series General Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Remote Enable Logic Low:					
$I_{ON/OFF}$ = 1.0mA	$V_{ON/OFF}$	0	-	1.2	V
$V_{ON/OFF}$ = 0.0V	$I_{ON/OFF}$	-	-	1.0	mA
Logic High:					
$I_{ON/OFF}$ = 0.0 $\mu$ A	$V_{ON/OFF}$	3.5	-	15	V
Leakage Current	$I_{ON/OFF}$	-	-	50	$\mu$ A
Isolation Capacitance	-	-	2200	-	pF
Isolation Resistance	-	10	-	-	M $\Omega$

### Module Specific Specifications

#### 5.5V/90A Module (FYVEA055x090xxx-x)

Parameter	Symbol	Min	Typical	Max	Unit
Input Current	$I_{in,Max}$	-	-	3.6	A
Quiescent Input Current (Typical $V_{in}$ )	$I_{in,Qsnt}$	-	30	45	mA
Standby Input Current	$I_{in,Stdby}$	-	5	8	mA
Efficiency (Typical $V_{in}$ ; $I_o$ ,max, $T_A$ = 25°C)	$\eta$	88.7	90.7	-	%
Output Voltage Set Point	$V_o$		5.5		V
Output Over Current Protection Set Point	$I_{o,cli}$	95.0	104.0	120.0	A
Output Over Voltage Protection Set Point	-	6.3	6.7	7.1	V
Output ripple frequency	-	196	206	216	KHZ
Output Ripple and Noise Voltage RMS	-		70	100	mVrms
Peak-to-peak (5 Hz to 20 MHz bandwidth, Typical $V_{in}$ )	-		120	250	mVp-p
External Load Capacitance	-	-	-	100,000	$\mu$ F

## FYVEA Series 180 – 400V Input Full Brick Converters

### 7V/90A Module (FYVEA070x090xxx-x)

Parameter	Symbol	Min	Typical	Max	Unit
Input Current	lin,Max	-	-	3.8	A
Quiescent Input Current (Typical Vin)	lin,Qsnt	-	25	35	mA
Standby Input Current	lin,Stdby	-	5	10	mA
Efficiency (Typical Vin; Io,max, TA = 25°C)	$\eta$	88.0	91.0	-	%
Output Voltage Set Point	Vo		7.0		V
Output Over Current Protection Set Point	Io,cli	100.0	110.0	115.0	A
Output Over Voltage Protection Set Point	-	8.0	8.5	8.8	V
Output ripple frequency	-	225	240	255	KHZ
Output Ripple and Noise Voltage					
RMS	-		23	45	mVrms
Peak-to-peak (5 Hz to 20 MHz bandwidth, Typical Vin)	-		113	225	mVp-p
External Load Capacitance	-	-	-	300,000	uF

\*For 7V output module, the output trim up range from 90% to 110%

### 12V/57A Module (FYVEA120x057xxx-x)

Parameter	Symbol	Min	Typical	Max	Unit
Input Current	lin,Max	-	-	5.1	A
Quiescent Input Current (Typical Vin)	lin,Qsnt	-	25	35	mA
Standby Input Current	lin,Stdby	-	5	10	mA
Efficiency (Typical Vin; Io,max, TA = 25°C)	$\eta$	90.0	92.0	-	%
Output Voltage Set Point	Vo		12.0		V
Output Over Current Protection Set Point	Io,cli	60.0	67.0	73.0	A
Output Over Voltage Protection Set Point	-	13.8	14.6	15.5	V
Output ripple frequency	-	225	240	255	KHZ
Output Ripple and Noise Voltage					
RMS	-		35	55	mVrms
Peak-to-peak (5 Hz to 20 MHz bandwidth, Typical Vin)	-		180	220	mVp-p
External Load Capacitance	-	-	-	50,000	uF

### 28V/28A Module (FYVEA280x028xxx-x)

Parameter	Symbol	Min	Typical	Max	Unit
Input Current	lin,Max	-	-	5.3	A
Quiescent Input Current (Typical Vin)	lin,Qsnt	-	30	40	mA
Standby Input Current	lin,Stdby	-	5	10	mA
Efficiency (Typical Vin; Io,max, TA = 25°C)	$\eta$	-	93.0	-	%
Output Voltage Set Point	Vo		28.0		V
Output Over Current Protection Set Point	Io,cli	32.5	34.5	35.0	A
Output Over Voltage Protection Set Point	-	33.0	35.0	36.0	V
Output ripple frequency	-	235	250	265	KHZ
Output Ripple and Noise Voltage					
RMS	-		30	50	mVrms
Peak-to-peak (5 Hz to 20 MHz bandwidth, Typical Vin)	-		150	250	mVp-p
External Load Capacitance	-	-	-	20,000	uF

### 36V/22A Module (FYVEA360x022xxx-x)

Parameter	Symbol	Min	Typical	Max	Unit
Input Current	lin,Max	-	-	6	A
Quiescent Input Current (Typical Vin)	lin,Qsnt	-	25	35	mA
Standby Input Current	lin,Stdby	-	5	10	mA
Efficiency (Typical Vin; Io,max, TA = 25°C)	$\eta$	91.0	93.0	-	%
Output Voltage Set Point	Vo		36.0		V
Output Over Current Protection Set Point	Io,cli	25.0	27.0	28.0	A
Output Over Voltage Protection Set Point	-	41.0	43.0	45.0	V
Output ripple frequency	-	235	250	265	KHZ
Output Ripple and Noise Voltage					
RMS	-		15	30	mVrms
Peak-to-peak (5 Hz to 20 MHz bandwidth, Typical Vin)	-		100	150	mVp-p
External Load Capacitance	-	-	-	10,000	uF

**48V/17A Module (FYVEA048x017xxx-x)**

Parameter	Symbol	Min	Typical	Max	Unit
Input Current	$I_{in,Max}$	-	-	5.5	A
Quiescent Input Current (Typical $V_{in}$ )	$I_{in,Qsnt}$	-	35	40	mA
Standby Input Current	$I_{in,Stdby}$	-	5	10	mA
Efficiency (Typical $V_{in}$ ; $I_{o,max}$ , $T_A = 25^{\circ}C$ )	$\eta$	-	93.0	-	%
Output Voltage Set Point	$V_o$		48.0		V
Output Over Current Protection Set Point	$I_{o,cli}$	17.5	19.5	22.0	A
Output Over Voltage Protection Set Point	-	53.0	56.0	59.0	V
Output ripple frequency	-	235	250	265	KHZ
Output Ripple and Noise Voltage					
RMS	-		25	45	mVrms
Peak-to-peak (5 Hz to 20 MHz bandwidth, Typical $V_{in}$ )	-		125	170	mVp-p
External Load Capacitance	-	-	-	4,800	$\mu F$

**Feature Descriptions**

**ON/OFF**

The converter can be turned on and off by changing the voltage between the ON/OFF pin and  $V_{in}(-)$ . The FYVEA Series of converters are available with positive logic and negative logic.

For the negative control logic, the converter is ON when the ON/OFF pin is at a logic low level and OFF when the ON/OFF pin is at a logic high level. For the positive control logic, the converter is ON when the ON/OFF pin is at a logic high level and OFF when the ON/OFF pin is at a logic low level.

With the internal pull-up circuitry, a simple external switch between the ON/OFF pin and  $V_{in}(-)$  can control the converter.

The logic low level is from 0V to 1.2V and the maximum sink current during logic low is 1mA. The external switch must be capable of maintaining a logic-low level while sinking up to this current. The logic high level is from 3.5V to 15V. The converter has an internal pull-up circuit that ensures the ON/OFF pin at a high logic level when the leakage current at ON/OFF pin is no greater than 50 $\mu A$ .

**Remote SENSE**

The remote SENSE pins are used to sense the voltage at the load point to accurately regulate the load voltage and eliminate the impact of the

voltage drop in the power distribution path.

SENSE(+) and SENSE(-) pins should be connected between the points where voltage regulation is desired. The voltage between the SENSE pins and the output pins must not exceed 0.5V.

$$[V_{out(+)} - V_{out(-)}] - [SENSE(+) - SENSE(-)] < 0.5V$$

When remote sense is not used, the SENSE pins should be connected to their corresponding output pins. If the SENSE pins are left floating, the converter will deliver an output voltage slightly higher than its specified typical output voltage.

**Output Voltage Adjustment (Trim)**

The trim pin allows the user to adjust the output voltage set point. To increase the output voltage, an external resistor is connected between the TRIM pin and SENSE(+). To decrease the output voltage, an external resistor is connected between the TRIM pin and SENSE(-). The output voltage trim range is 80% to 110% of the specified typical output voltage. The circuit configuration for trim down operation is shown in Figure 1.

To decrease the output voltage, the value of the external resistor should be.

$$R_{down} = \left( \frac{202.92}{\Delta} - 7.14 \right) (k\Omega)$$

Where

$$\Delta = \left( \frac{|V_{nom} - V_{adj}|}{V_{nom}} \right) \times 100$$

$V_{nom}$  = Typical Output Voltage

$V_{adj}$  = Adjusted Voltage

The circuit configuration for trim up operation is shown in Figure 2. To increase the output voltage, the value of the resistor should be:

$$R_{up} = \left( \frac{2.05V_o(100 + \Delta)}{1.225\Delta} - \frac{202.92}{\Delta} - 7.14 \right) (k\Omega)$$

Where

$V_o$  = Typical Output Voltage

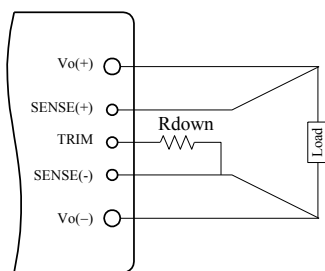


Figure 1. Circuit to Decrease Output Voltage

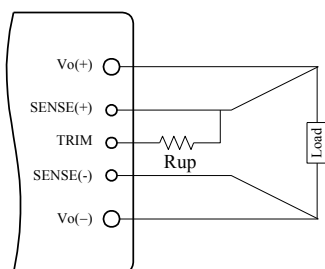


Figure 2. Circuit to Increase Output Voltage

### Output Over-Current Protection (OCP)

This converter can be ordered in either latch-off or auto-restart version upon OCP, OVP, and OTP.

With the latch-off version, the converter will latch off when the load current exceeds the limit. The converter can be restarted by toggling the ON/OFF switch or recycling the input voltage.

With the auto-restart version, the converter will operate in a hiccup mode (repeatedly try to restart) until the cause of the over-current condition is cleared.

### Output Over-Voltage Protection (OVP)

With the latch-off version, the converter will latch off when the output voltage exceeds the limit. The converter can be restarted by toggling the ON/OFF switch or recycling the input voltage.

With the auto-restart version, the converter will operate in a hiccup mode (repeatedly try to restart) until the cause of the over-voltage condition is cleared.

### Over Temperature Protection (OTP)

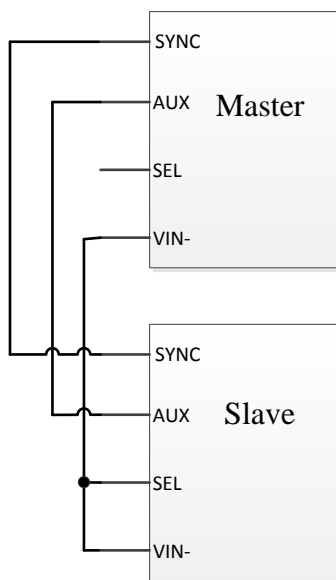
With the latch-off version, the converter will shut down and latch off if an over-temperature condition is detected. The converter has a temperature sensor located at a carefully selected position in the converter circuit board, which represents the thermal condition of key components of the converter. The thermal shutdown circuit is designed to turn the converter off when the temperature at the sensor reaches 120°C. The module can be restarted by toggling the ON/OFF switch or recycling the input voltage.

With the auto-restart version, the converter will resume operation after the converter cools down.

### Internal Clock and External Synchronization

When an FYVEA converter is operating by itself, its SEL pin should be left open and the PWM switching actions are synchronized to its internal synchronous clock.

To synchronize multiple FYVEA converters in a system, one of the converters is selected as the master converter and its SEL pin shall be left open while all other slave converters shall have their SEL pins tied to input negative ( $V_{in-}$ ). All AUX pins shall be tied together. Figure 3 shows two converters synchronized to the internal synchronous clock of the master converter.

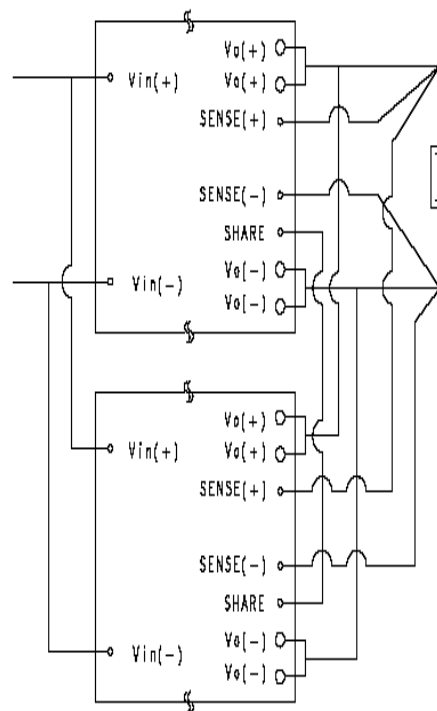


**Figure 3.** Two converters synchronized to internal synchronous clock of the master converter

FYVEA converters can also be synchronized to an external clock connected to the SYNC pins of all the converters. The SEL pins of all the converters shall be tied to input negative (Vin-). It is important to ensure that the external clock always presents and is stable during the operation of the power converter. An unstable external clock may cause permanent damage to the converter. The external clock should satisfy the requirements listed in Module Specific Specifications table.

### Load Current Sharing (Paralleling)

For the parallel operation of multiple converters with load sharing, SHARE pins of all converters should be connected together. It is suggested to have a copper plane on the system board for Vin(-) to reduce the ground noise impact on the current share accuracy. The loop formed by the trace connecting the SHARE pins and the Vin(-) shall be minimized to avoid noise coupling into the current sharing circuitry. A typical current sharing/paralleling scheme is shown in Figure4.



**Figure 4.** Circuit Configuration for Active Current Sharing

Up to eight FYVEA converters can operate in parallel to share the load current. When the beat frequency of converters in parallel is a concern, synchronization among the converters is often the choice.

AUX pin is an internal bias for synchronous clock, and it can also be used as a status indicator when the converter is not running in synchronized mode.

In applications where three or more converters are in synchronization, it is a good practice to choose a converter with relatively short distances to other converters as the master.

### Design Considerations

As with any DC/DC converter, the stability of the FYVEA converters may be compromised if the source impedance is too high or inductive. It's desirable to keep the input source ac-impedance as low as possible. Although the converters are designed to be stable without adding external input capacitors for typical source impedance, it is recommended to add 10 μF low ESR electrolytic capacitors at the

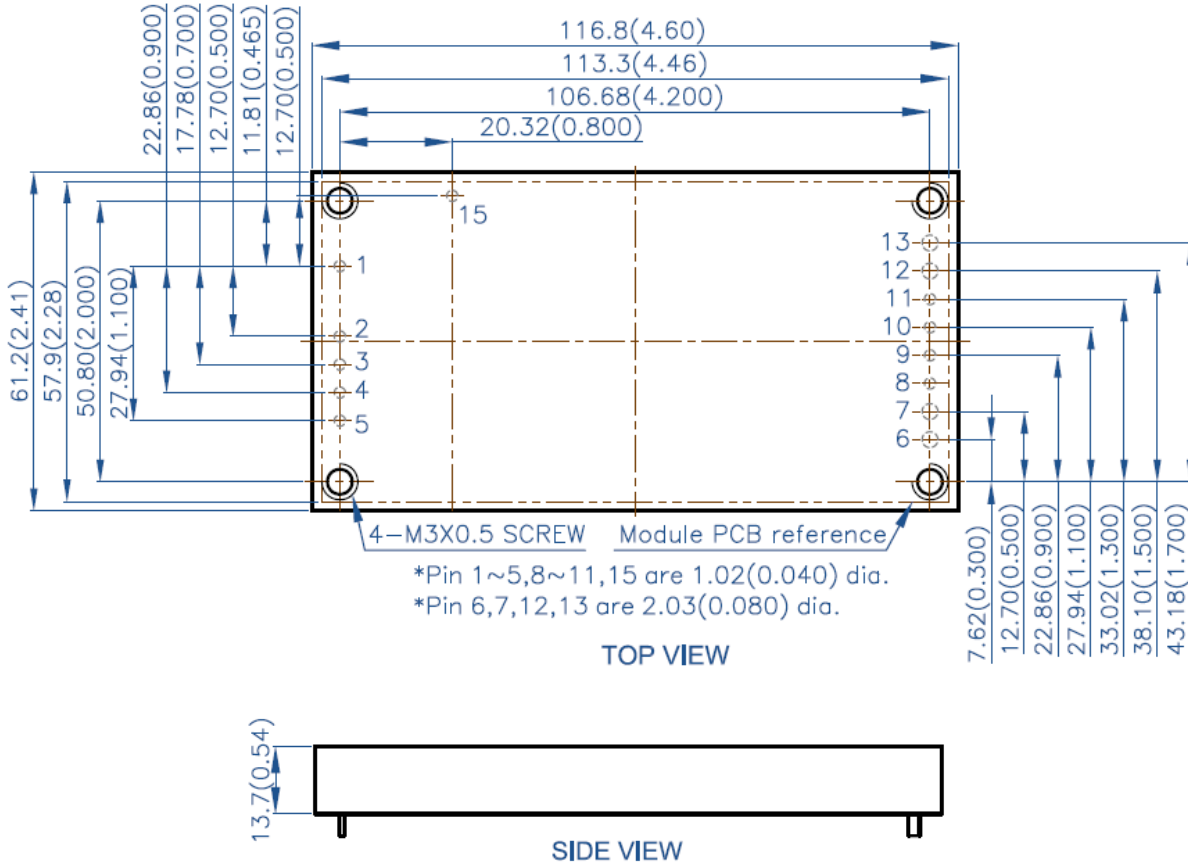
input of the converter for each 100W output power, which reduces the potential negative impact of the source impedance on the converter stability. These electrolytic capacitors should have sufficient RMS current rating over the operating temperature range.

The converter is designed to be stable without additional output capacitors. To further reduce the output voltage ripple or improve the transient response, additional output capacitors are often used in applications. When additional output capacitors are used, a combination of ceramic capacitors and tantalum/polymer capacitors shall be used to provide good filtering while assuring the stability of the converter.

# FYVEA Series 180 – 400V Input Full Brick Converters

## Mechanical Information

Potted, metal case (with AUX option)



Pin	Name	Function
1	Vin(+)	Positive input
2	ON/OFF	Remote control
3	SEL	Clock select
4	SYNC	External sync signal input
5	Vin(-)	Negative input
6	Vout(-)	Negative output
7	Vout(-)	Negative output
8	SHARE	Current share
9	SENSE(-)	Negative remote sense
10	TRIM	Output voltage adjust
11	SENSE(+)	Positive remote sense
12	Vout(+)	Positive output
13	Vout(+)	Positive output
15	AUX (Optional)	Supply pin for internal synchronous clock

### Notes:

- All dimensions in mm (inches)  
Tolerances:  $x \pm .5$  ( $.xx \pm 0.02$ )  
 $.xx \pm .25$  ( $.xxx \pm 0.010$ )
- Input and function pins are 1.02mm (0.040") dia. with +/- 0.10mm (0.004") tolerance. The recommended diameter of the receiving hole is 1.42mm (0.056").
- Output pins are 2.03 mm (0.080") dia. with +/- 0.10mm (0.004") tolerance. The recommended diameter of the receiving hole is 2.44mm (0.096").
- All pins are coated with 90%/10% solder, Gold, or Matte Tin finish with Nickel underplating.
- Workmanship meets or exceeds IPC-A-610 Class II.
- Torque applied on screw should not exceed 6in-lb. (0.7 Nm).
- Baseplate flatness tolerance is 0.10mm (0.004") TIR for surface.