

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED, N-CHANNEL,
SILICON, TYPES 2N7648 QUALITY LEVELS JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device. Provisions for radiation hardness assurance (RHA) to two radiation levels ("R" and "F") are provided for JANTXV and JANS product assurance level.

1.2 Package outlines. The device package outlines are as follows: TO-257AA (D5) in accordance with [figure 1](#), a modified tab-less TO-257AA (T3) in accordance with [figure 2](#), and a surface mount TO-276AA (U3, U3C) in accordance with [figure 3](#) for all encapsulated device types.

1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$	I_{D2} $T_C = +100^\circ\text{C}$	I_S	I_{DM} (5)	T_J and T_{STG}	V_{ISO} 70,000 ft. altitude
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A</u> (pk)	<u>°C</u>	<u>V dc</u>
2N7648U3, 2N7648U3C	75	1.56	1.67	100	100	±20	35	22	35	140	-55 to +150	250
2N7648T3, 2N7648D5	75	1.56	1.67	100	100	±20	30	22	30	120		

(1) Derate linearly by 0.6 W/°C for $T_C > +25^\circ\text{C}$.

(2) See [figure 4](#), thermal impedance curves.

(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(4) See [figure 5](#), maximum drain current graph.

(5) $I_{DM} = 4 \times I_{D1}$; I_{D1} as calculated by footnote (3).

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1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0\text{mA dc}$	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0\text{ mA dc}$	Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80\%$ of rated V_{DS}	Max $r_{DS(on)}$ (1) $V_{GS} = 12\text{V}, I_D = I_{D2}$		E_{AS}
				$T_J = +25^\circ\text{C}$	$T_J = +150^\circ\text{C}$	
	<u>V dc</u>	<u>V dc</u> Min Max	<u>$\mu\text{A dc}$</u>	<u>Ω</u>	<u>Ω</u>	<u>mJ</u>
2N7648U3, 2N7648U3C	100	2.0 4.0	1.0	0.034	0.062	605
2N7648T3, 2N7648D4	100	2.0 4.0	1.0	0.035	0.064	605

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and for a list of available PINs.

1.5.1 JAN certification mark and quality level. The only quality level designators for encapsulated devices that are applicable for this specification sheet are the quality levels "JANTXV" and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R" and "F".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

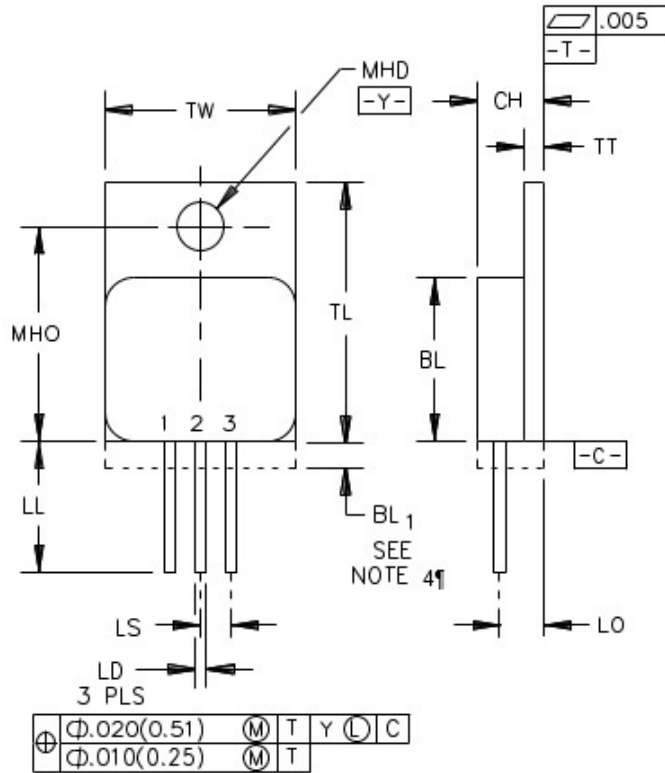
1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7648".

1.5.4 Suffix letters. The following suffix letters are incorporated in the PIN for this specification sheet:

T3	Indicates a metal lidded 3 terminal leaded package similar to a TO-257AA (see figure 1)
D5	Indicates a metal lidded 3 terminal leaded package similar to a tab-less TO-257AA (see figure 2)
U3	Indicates a metal lidded 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 3).
U3C	Indicates a ceramic lidded 3 pad surface mount package similar to a TO-276AA (SMD-0.5) (see figure 3).

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

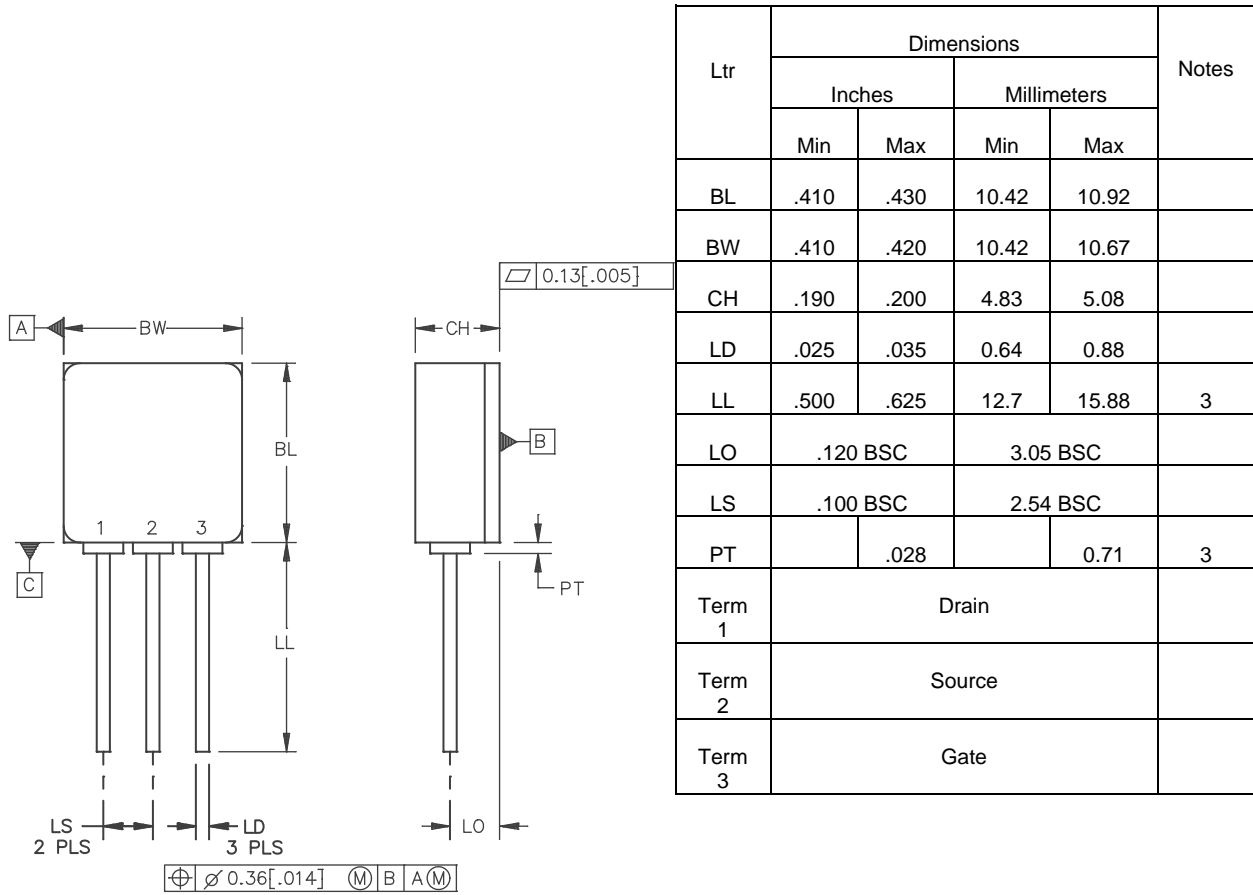
Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
BL ₁		.033		0.84
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.600	.650	15.24	16.51
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Drain			
Term 2	Source			
Term 3	Gate			



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 1. Dimensions and configuration, TO-257AA (T3).

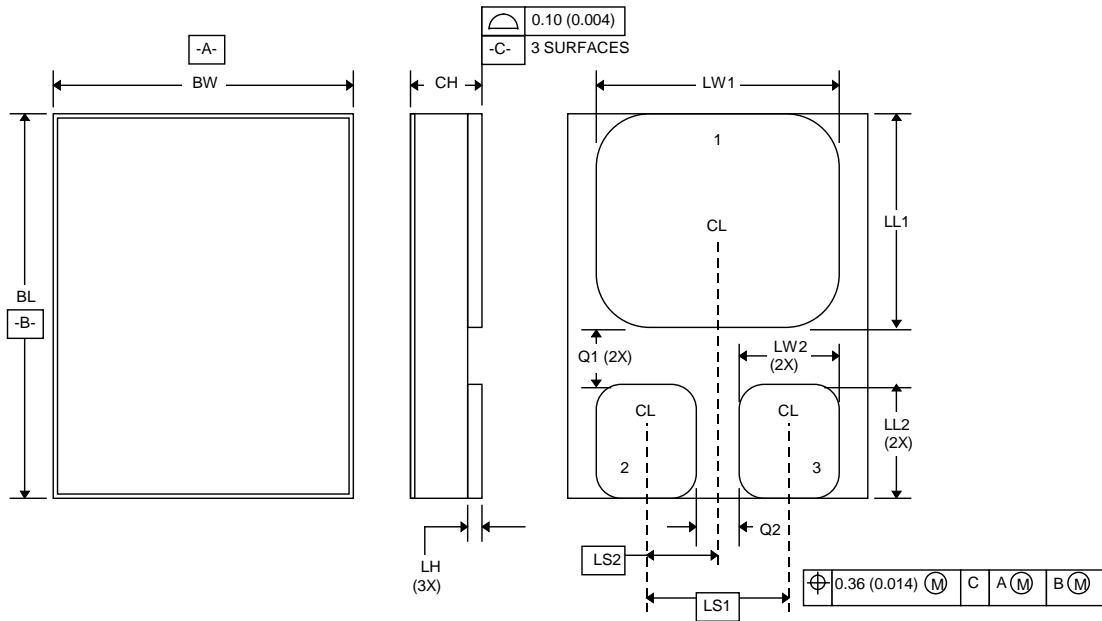


NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness (PT) of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 2. Physical dimensions for TO-257AA modified (tab-less package metal lid) D5.

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH (for U3)		.124		3.15
CH (for U3C)		.134		3.39
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimension are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate, and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
5. Metal lid: U3 suffix; Ceramic lid: U3C suffix.

FIGURE 3. Dimensions and configuration (TO-276AA, SMD-0.5), with metal lid or ceramic lid.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figures 1](#) (T3, TO-257AA with metal lid), [2](#) (TO-257AA with metal lid and tab-less), and [3](#) (U3, U3C, surface mount TO-276AA) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Multiple chip construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.4.3 Silicone Die coating. Qualified silicone die coating is permitted with the approval of the qualifying activity

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate shall be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and [tables I and II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see [table III](#) and [table IV](#)). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of [MIL-STD-750](#) that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with [table II](#). SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

4.3 Screening of encapsulated devices. Screening of packaged devices shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DS(ON)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DS(ON)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.
17	For TO-257AA (T3 and D5 suffixes) and TO-276AA (U3 suffix) packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.	For TO-257AA (T3 and D5 suffixes) and TO-276AA (U3 suffix) packages: Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} and $V_{GS(th)1}$ shall be invoked
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 24$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current $I_{AS} = I_{D2}$.
- b. Inductance:..... $\left[\frac{2E_{AS}}{(I_{D2})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200 \Omega$.
- d. Supply voltage (V_{DD})..... $V_{DD} = 25$ V dc, up to rated V_{DS} .
- e. Peak gate voltage (V_{GS}) 12 V, up to maximum rated V_{GS} .
- f. Initial case temperature $T_c = +25^\circ\text{C} +10^\circ\text{C}, -5^\circ\text{C}$.
- g. Number of pulses to be applied..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 30 - 60 μ s max. See [table III](#), group E, subgroup 4 herein.

4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and be evaluated for root cause and lot integrity.

4.3.5 Dielectric withstanding voltage.

- a. Magnitude of test voltage.....600V dc.
- b. Duration of application of test voltage.....15 seconds (min).
- c. Points of application of test voltage.....All leads to case (bunch connection).
- d. Method of connection.....Mechanical
- e. Kilovolt-ampere rating of high voltage source.....1,200 V.1,0 mA (min).
- f. Maximum leakage current.....1.0 mA.
- g. Voltage ramp up time.....500 V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#), and as follows.

4.4.2.1 Quality level JANS (table E-VIA of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM).
B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	Intermittent operation life, condition D, $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$; $T_A = +175^\circ\text{C}$, t = 24 hours minimum; or $T_A = +150^\circ\text{C}$, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated}$; $T_A = +175^\circ\text{C}$, t = 120 hours minimum; or $T_A = +150^\circ\text{C}$, t = 240 hours minimum.
B5	2037	Test condition D.

4.4.2.2 Quality level JANTXV (table E-VIB of [MIL-PRF-19500](#)).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, $t_{on} = 30$ seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Terminal strength is not applicable to the TO-276AA (U3 and U3C) package
C3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	See 4.3.3, $R_{\theta JC} = 1.67$ °C/W.
C6	1042	Intermittent operation life, condition D, $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of [MIL-PRF-19500](#) and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table III](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

MIL-PRF-19500/775

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	Bias condition C, $V_{GS} = 0$ V, $I_D = 1$ mA dc	$V_{(BR)DSS}$	100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1$ mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$ V	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$ V dc, bias condition C, $V_{DS} = 80$ percent of rated V_{DS} ,	I_{DSS1}		1.0	μA dc
Static drain to source on-state resistance 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5	3421	$V_{GS} = 12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.034 0.035	Ω Ω
Forward voltage	4011	$V_{GS} = 0$ V dc, condition A, $I_D = I_{D1}$	V_{SD}		1.2	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation $T_C = T_J = +125^\circ\text{C}$						
Gate current	3411	$V_{GS} = \pm 20\text{ V dc}$, bias condition C, $V_{DS} = 0\text{ V}$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0\text{ V dc}$, bias condition C, $V_{DS} = 80\text{ percent of rated } V_{DS}$	I_{DSS2}		10	$\mu\text{A dc}$
Static drain to source on-state resistance 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5	3421	$V_{GS} = 12\text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$		0.061	Ω
					0.063	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation $T_C = T_J = -55^\circ\text{C}$						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)3}$		5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = I_{D2}$, $V_{DD} = 15\text{ V dc}$ (see 4.5.1)	g_{FS}	14		S
Switching Time Tests						
Turn-On Delay Time 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5	3472	$I_D = I_{D1}$, $V_{GS} = 12\text{VDC}$, $R_G = 7.5\Omega$, $V_{DD} = 50\text{ percent Rated } V_{DS}$	$t_{d(on)}$		25	
					25	
Rise Time 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5			t_r		26	
					35	
Turn-Off Delay Time 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5			$t_{d(off)}$		38	
					45	
Fall Time 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5			t_f		27	
					30	
<u>Subgroup 5</u>						
Safe operating area test	3474	See figure 4 ; $t_p = 10\text{ ms min.}$ $V_{DS} = 80\text{ percent of max. rated } V_{DS}$				
Electrical measurements		See table 1 , subgroup 2				
<u>Subgroup 6</u>						
Not applicable						

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 7</u>						
Gate charge	3471	Condition B, $I_D = I_{D1}$, $V_{GS} = 12$ V dc $V_{DD} = 50$ percent of rated V_{DS}	Q_G			nC
On-state gate charge and turn-off gate charge 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5					48 44	
Gate to source charge (turn-on and turn-off) 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5				Q_{GS}	25 20	
Gate to drain charge (turn-on and turn-off) 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5				Q_{GD}	9 15	
Reverse recovery time	3473	Condition A, $di/dt = -100$ A/ μ s, $V_{DD} \leq 50$ V, $I_D = I_{D1}$	t_{rr}		210	ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point measurements, this test is required for the following subgroups:
 Group B, subgroups 2 and 3 (JANTXV).
 Group B, subgroups 3 and 4 (JANS).
 Group C, subgroup 2 and 6.
 Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits		Unit
	Method	Conditions		R and F		R and F		
				Min	Max	Min	Max	
<u>Subgroup 1</u>								
Not applicable								
<u>Subgroup 2</u>		$T_C = + 25^\circ\text{C}$						
Steady-state total dose irradiation (V_{GS} bias) <u>4/</u>	1019	$V_{GS} = 12 \text{ V};$ $V_{DS} = 0$						
Steady-state total dose irradiation (V_{DS} bias) <u>4/</u>	1019	$V_{GS} = 0; V_{DS} = 80$ percent of rated V_{DS} (pre-irradiation)						
End-point electricals:								
Breakdown voltage, drain to source 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5	3407	Bias condition C, $V_{GS} = 0;$ $I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	100		100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ $I_D = 1 \text{ mA}$	$V_{GS(th)1}$	2.0	4.0	2.0	4.0	V dc
Gate current	3411	Bias condition C, $V_{GS} = +20 \text{ V}; V_{DS} = 0$	I_{GSSF1}		100		100	nA dc
Gate current	3411	Bias condition C, $V_{GS} = -20 \text{ V}; V_{DS} = 0$	I_{GSSR1}		-100		-100	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS} (pre-irradiation)	I_{DSS}		1.0		1.0	μA dc
Static drain to source on-state voltage 2N7648U3, 2N7648U3C 2N7648T3, 2N7648D5 <u>5/</u>	3405	$V_{GS} = 12 \text{ V}; I_D = I_{D2}$ condition A, pulsed (see 4.5.1)	$V_{DS(on)}$		0.748 0.770		0.748 0.770	V dc V dc
Forward voltage source drain diode	4011	Bias condition A, $V_{GS} = 0;$ $I_D = I_{D1}$	V_{SD}		1.2		1.2	V dc

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

5/ Group D samples are built and tested in T0-3 packages. The equivalent pre-radiation and post radiation limit for $V_{DS(on)}$ in the T0-3 package is 0.792Vdc.

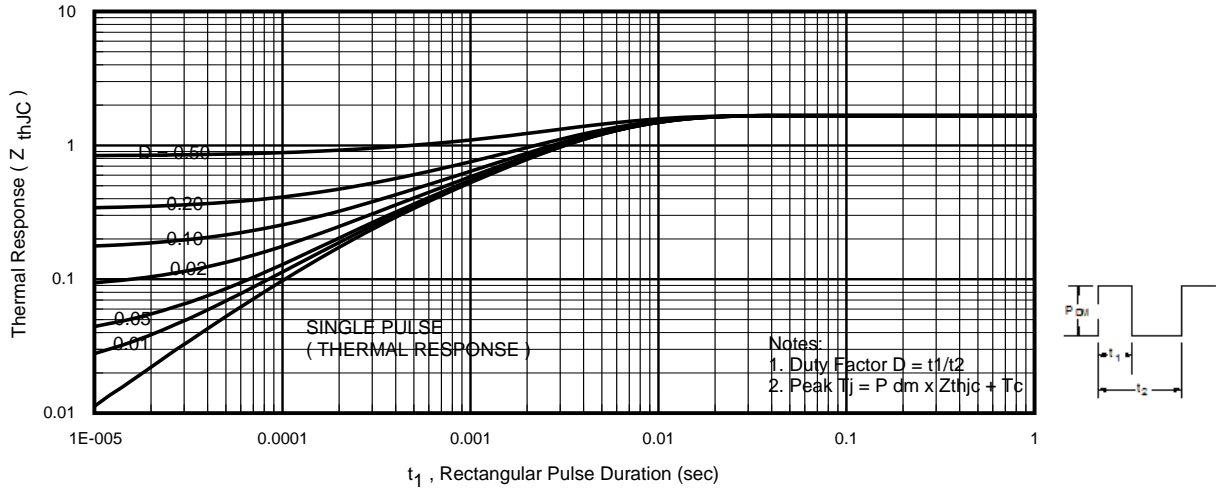
TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	-55°C to +150°C, 500 cycles	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I , subgroup 2 herein.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 3</u>			n = 45, c = 0
Not Applicable			
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 5</u>			
Not Applicable			
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		

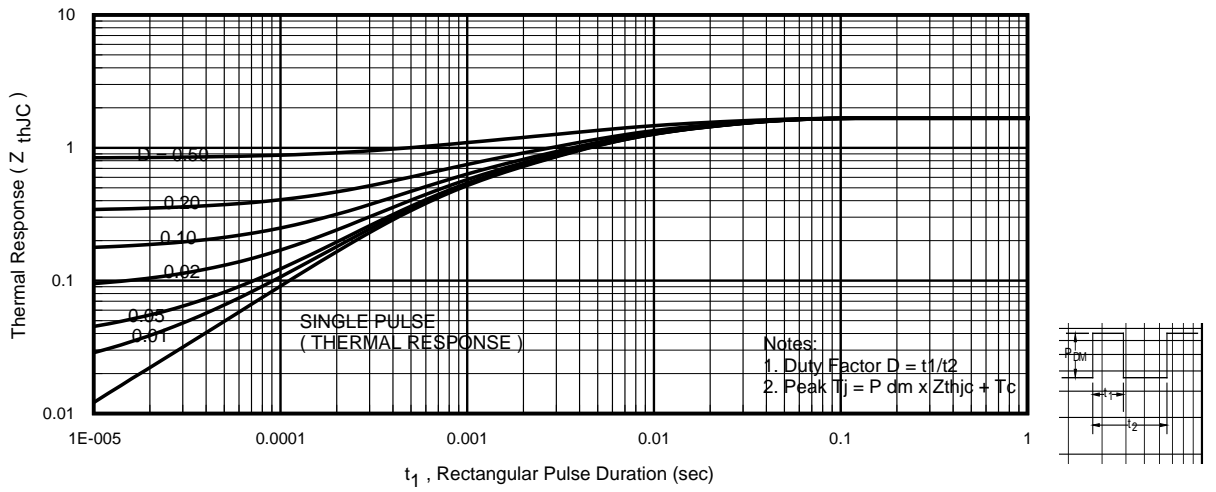
1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level linear energy transfer (LET) is sufficient to qualify all lower level LETs.



2N7648U3, 2N7648U3C.



2N7648T3, 2N7648D5

FIGURE 4. Thermal response curve

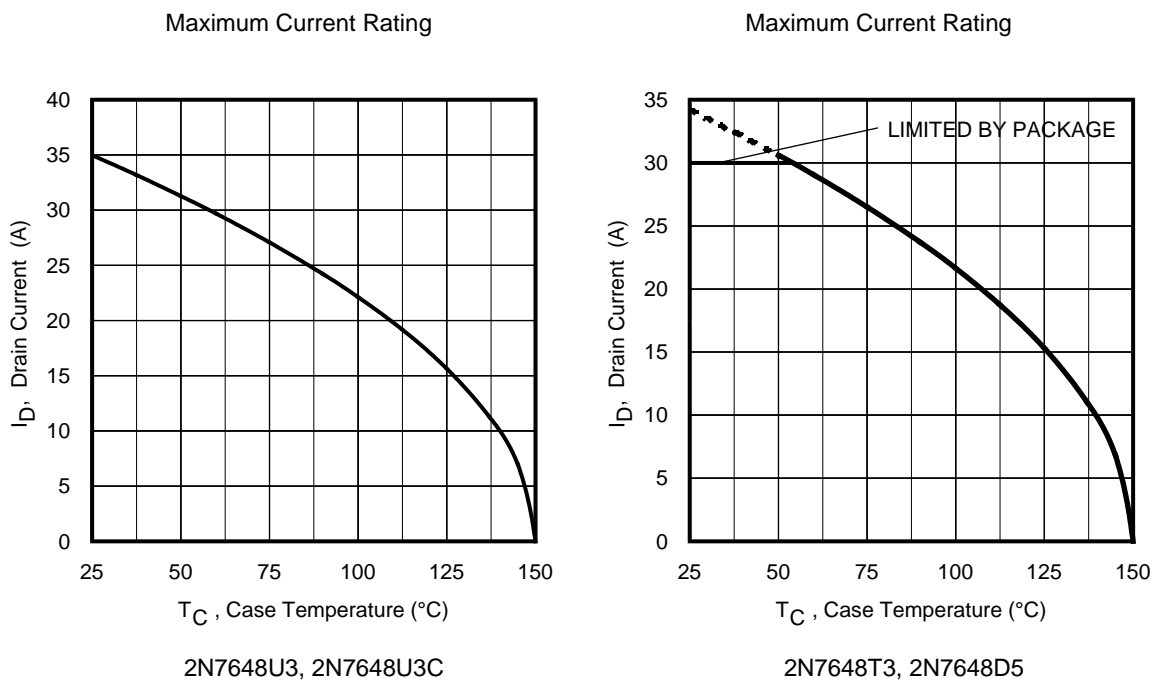
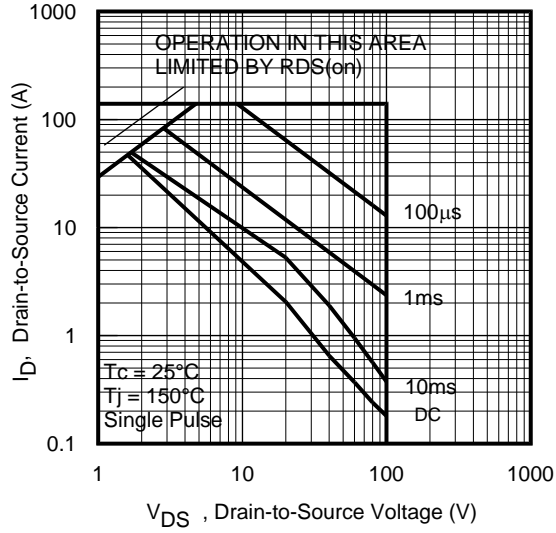
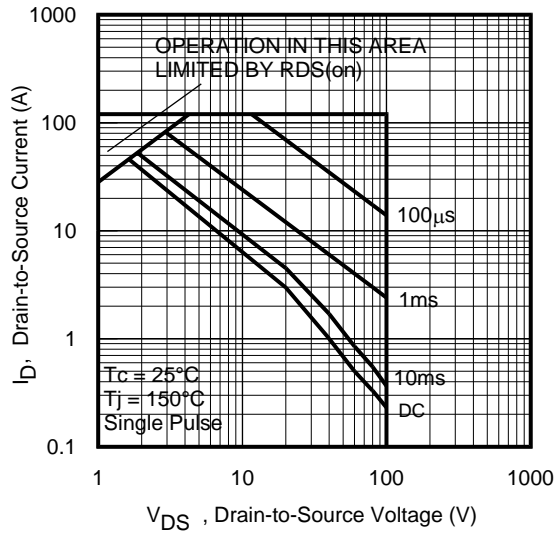


FIGURE 5. Maximum drain current versus case temperature graphs.



2N7648U3, 2N7648U3C



2N7648T3, 2N7648D5

FIGURE 6. Safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

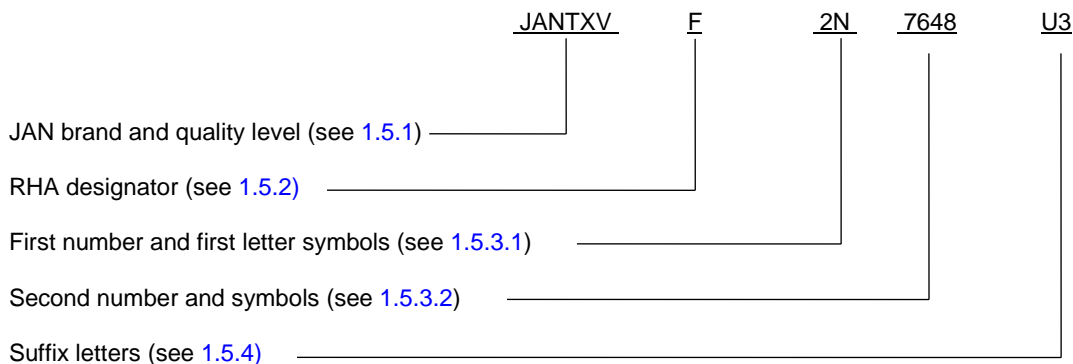
- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.6.
- e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.
- f. If SEE testing data is desired, it should be specified in the contract or order.
- g. If specific SEE characterization conditions are desired (see section 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN) (without JAN and RHA prefix). This information in no way implies that manufacturer's PINs are substitutable for the military PIN.

Preferred types military PIN	Commercial PIN
2N7648U3 2N7648U3C 2N7648T3 2N7648D5	IRHNJ9A7130 IRHNJC9A7130 IRHYS9A7130CM IRHYB9A7130CM

6.5 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.6 List of PINs. The following is a list of possible PINs (without JAN brand) available on this specification sheet.

JANTXVF2N7648U3	JANTXVF2N7648U3C	JANTXVF2N7648T3	JANTXVF2N7648D5
JANTXVR2N7648U3	JANTXVR2N7648U3C	JANTXVR2N7648T3	JANTXVR2N7648D5
JANSF2N7648U3	JANSF2N7648U3C	JANSF2N7648T3	JANSF2N7648D5
JANSR2N7648U3	JANSR2N7648U3C	JANSR2N7648T3	JANSR2N7648D5

6.7 Application data.

6.7.1 Manufacturer specific irradiation data. Each manufacturer qualified to this specification sheet has characterized its devices to the requirements of [MIL-STD-750](#) method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

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TABLE IV. Manufacturers characterization conditions.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210	SEE <u>1/</u>	1080	See MIL-STD-750 method 1080 and figure 7	3 devices
	Pre SEE Electrical measurements		I _{GSSF1} , I _{GSSR1} , and I _{DSS1} in accordance with table I, subgroup 2	
	SEE irradiation		Fluence = 3E5 ±20 percent ions/cm ² Flux = 4E3 to 4E4 ions/cm ² /sec, temperature = 25 ±5°C Surface LET = 37 MeV-cm ² /mg ±5%, range = 50 μm ±7.5%, energy = 418 MeV ±7.5% In-situ bias conditions: V _{DS} = 100 V and V _{GS} = -10 V (Typical 4.98 MeV/Nucleon at Texas A & M Cyclotron)	
	2N7648U3, 2N7648U3C, 2N7648T3, 2N7648D5			
	Post SEE Electrical measurements	I _{GSSF1} , I _{GSSR1} , and I _{DSS1} in accordance with table I, subgroup 2		
	SEE <u>1/</u>	1080	See MIL-STD-750 method 1080	3 devices
Pre SEE Electrical measurements	I _{GSSF1} , I _{GSSR1} , and I _{DSS1} in accordance with table I, subgroup 2			
SEE irradiation	Fluence = 3E5 ±20 percent ions/cm ² Flux = 4E3 to 4E4 ions/cm ² /sec, temperature = 25 ±5°C			
2N7648U3, 2N7648U3C, 2N7648T3, 2M7648D5	Surface LET = 59.8 MeV-cm ² /mg ±5%, range = 60.8 μm ±7.5%, energy = 755MeV ±7.5% In-situ bias conditions: V _{DS} = 100 V and V _{GS} = -10 V; Typical 5.85 MeV/Nucleon at Texas A & M Cyclotron)			
Post SEE Electrical measurements	I _{GSSF1} , I _{GSSR1} , and I _{DSS1} in accordance with table I, subgroup 2			

TABLE IV. Manufacturers characterization conditions - continued.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210	SEE 1/ Pre SEE Electrical measurements SEE irradiation 2N7648U3, 2N7648U3C, 2N7648T3, 2N7648D5 Post SEE Electrical measurements	1080	See MIL-STD-750 method 1080 and figure 7 I _{GSSF1} , I _{GSSR1} , and I _{DSS1} in accordance with table 1, subgroup 2 Fluence = 3E5 ±20 percent ions/cm ² Flux = 4E3 to 4E4 ions/cm ² /sec, temperature = 25 ±5°C Surface LET = 89.75 MeV-cm ² /mg ±5%, range = 82 µm ±7.5%, energy = 1518 MeV ±7.5% In-situ bias conditions: V _{DS} = 100 V and V _{GS} = 0 V V _{DS} = 100 V and V _{GS} = -1 V V _{DS} = 100 V and V _{GS} = -5 V V _{DS} = 100 V and V _{GS} = -10 V (Typical 7.7 MeV/Nucleon at Texas A & M Cyclotron) I _{GSSF1} , I _{GSSR1} , and I _{DSS1} in accordance with table 1, subgroup 2	3 devices
Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} parameters were examined before and following SEE irradiation to determine acceptability for each bias conditions. Other test conditions in accordance with [table 1](#), subgroup 2, may be performed at the manufacturer's option.

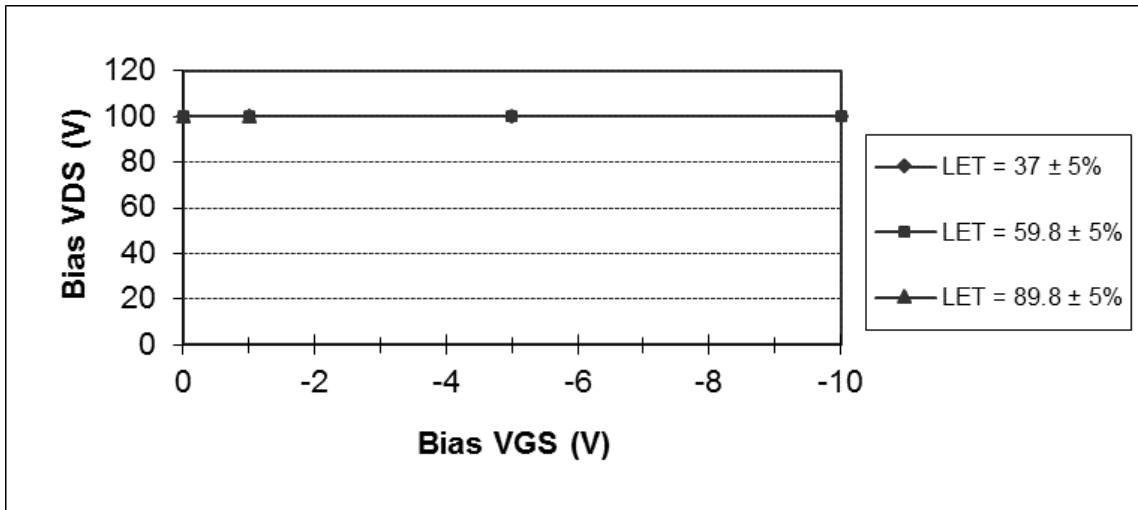


FIGURE 7. SEE safe operating area graph.

6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2018-044)

Review activity:
 Army - AV, MI
 Air Force - 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.