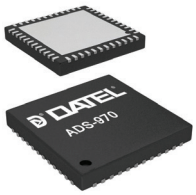
# ADS-970

16-Bit, 125MSPS, Differential, A/D Converters




## FEATURES

- Single supply 1.8V operation
- 125MSPS sampling rate
- JESD204B high-speed data interface
- SNR : 78.0 dBFs Fin = 30MHz
- SFDR : 94.0 dBc Fin = 30MHz
- Programmable built-in test patterns
- Multi-Chip Time Alignment and Deterministic Latency Support (JESD204B Device Subclass 2)
- SPI programmable debugging features and test patterns
- Power consumption 700mW
- 48-pin 7mm x 7mm Leadless Plastic Quad Flat Package.

## PRODUCT OVERVIEW

The ADS-970 is a low-power, high-performance, 16-bit, serial output analog-to-digital converter. Designed on a standard CMOS process, this converter supports sampling rates of up to 125MSPS. A proprietary architecture design minimizes power consumption while providing exceptional dynamic performance and optimal DC performance-vs-power trade-off.

This high-speed converter utilizes the industry standard JESD204B-compliant, high speed serial output link, offering data rates up to 4.3 Gbps per lane and multiple packing modes. The SERDES transmitter output uses two lanes to transmit the conversion data as well as a deterministic latency digital output scheme and a multi-chip time alignment option for complex synchronization requirements.

The serial peripheral interface (SPI) port provides an extensive array of configurability for the JESD204B transmitter including direct register access to the internal link and transport-layer test patterns. The SPI port also affords the user the control of numerous additional features such as the fine offset and gain adjustments of the two ADC cores as well as the programmable clock divider that allows both 2x and 4x harmonic clocking.

The ADC-970 is available in a space-saving 7mm x 7mm, 48-pin Leadless Plastic Quad Flat Package. This package features a thermal pad for improved thermal performance and is specified over an extended temperature range of (-40°C to +105°C). Military temperature range (-55°C to +125°C) devices are available.

## APPLICATIONS

- High-Speed /Performance Data Acquisition
- Radar and Satellite Antenna Array Processing
- High-Speed Medical Imaging
- Broadband Communications and Microwave Receivers

## BLOCK DIAGRAM

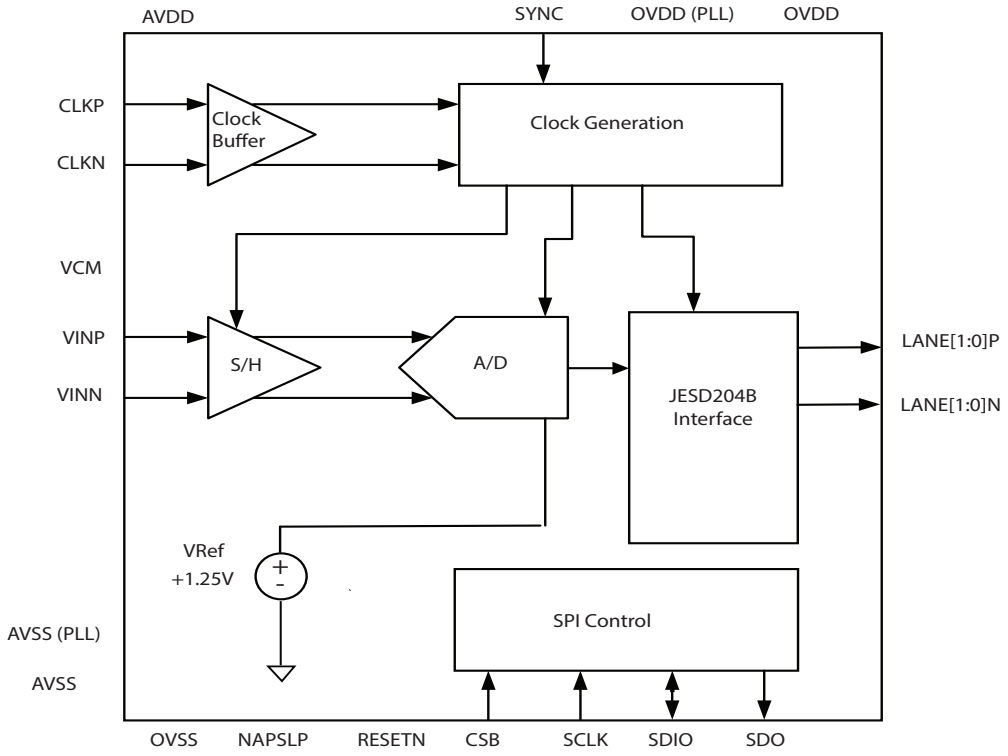



Figure 1. ADS-970 Functional Block Diagram

| ABSOLUTE MAXIMUM RATINGS | | |
|---|---|---|
| PARAMETERS | LIMITS | UNITS |
| AVDD to AVSS | -0.4 to 2.1 | V |
| OVDD to OVSS | -0.4 to 2.1 | V |
| AVSS to OVSS | -0.3 to 0.3 | V |
| Analog Inputs to AVSS | -0.4 to AVDD + 0.3 | V |
| Clock Inputs to AVSS | -0.4 to AVDD + 0.3 | V |
| Logic Input to AVSS | -0.4 to OVDD + 0.3 | V |
| Logic Inputs to OVSS | -0.4 to OVDD + 0.3 | V |
| Latchup (Tested per JESD-78C;Class 2,Level A) | 100 | mA |

| PHYSICAL / ENVIRONMENTAL | | |
|---|---|---|
| PARAMETERS | LIMITS | UNITS |
| θja (°C/W) | 24 | °C/W |
| θjc MSOP package | 0.4 | °C/W |
| Storage Temperature Range | -65 to +150 | °C |
| Junction Temperature | +150 | °C |

1. θJA is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
2. θJC, the "case temp" location is the center of the exposed metal pad on the package underside.

## FUNCTIONAL SPECIFICATIONS [1]

A VDD = 1.8V, OVDD = 1.8V , Ain = -2dBFS, $F_S$ = 125MHz, @ 25°C unless otherwise specified.

| ANALOG INPUTS | TEST CONDITION | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Full-Scale Analog Input Range | | 1.95 | 2.03 | 2.22 | V-pp |
| Input Resistance | | | 300 | | Ω |
| Input Capacitance | | | 10.7 | | pF |
| Full Scale Range Temp. Drift | | | 68 | | ppm/°C |
| Input Offset Voltage | | -5.0 | ±1 | 5.0 | mV |
| Gain Error | | | 1 | | % |
| Common-Mode Output Voltage | | | 0.94 | | V |
| Common Mode Input Current (per pin) | | | 12.0 | | µA/MSPS |
| **DYNAMIC PERFORMANCE** | | | | | |
| Differential Nonlinearity | | -0.99 | ±0.14 | | LSB |
| Integral Nonlinearity | | | ±9.0 | | LSB |
| Minimum Conversion Rate | | | | 100 | MSPS |
| Maximum Conversion Rate | | 125 | | | MSPS |
| Signal-to-Noise Ratio | Fin = 30MHz | | 78.5 | | dBFS |
| Signal-to-Noise and Distortion | Fin = 30MHz | | 77.5 | | dBFS |
| Spurious-Free Dynamic Range | | | 94 | | dBc |
| Spurious-Free Dynamic Range Excluding 1st and 2nd harmonics | | | 100 | | dBc |
| Effective Number of Bits | Fin = 30MHz | | 12.6 | | Bits |
| Intermodulation Distortion | Fin = 70MHz | | 96 | | dBFS |
| Word Error Rate | | | $10^{-13}$ | | |
| Full Power Bandwidth | | | 620 | | MHz |
| **DIGITAL I/O** | | | | | |
| Input Current High (RESETN) | VIN = 1.8V | | 1 | 10 | µA |
| Input Current Low (RESETN) | VIN = 0V | -25 | -12 | -7 | µA |
| Input Current High (SDIO, SCL, SDA SCLK) | VIN = 1.8V | | 4 | 12 | µA |
| Input Current Low (SDIO, SCL, SDA SCLK) | VIN = 0V | -600 | -400 | -300 | µA |
| Input Current High (CSB) | VIN = 1.8V | 40 | 52 | 70 | µA |
| Input Current Low (CSB) | VIN = 0V | | 1 | 10 | µA |
| Input Voltage High (SDIO, RESETN) | | 1.17 | | | V |
| Input Voltage Low (SDIO, RESETN) | | | | 0.63 | V |
| Input Current High (NAPSLP, CLKDIV) | | 19 | 25 | 30 | µA |
| Input Current High (NAPSLP, CLKDIV) | | --30 | -25 | -19 | µA |
| Input Capacitance | | | 4 | | pF |
| LVDS INPUTS (SYNCP, SYNCN) | | | | | |
| Input Common Mode Range | | 825 | | 1575 | mV |
| Input Differential Swing (peak-to-peak, single-ended) | | 250 | | 450 | mV |
| Input Pull-up and Pull-down Resistance | | | 100 | | kΩ |
| CML OUTPUTS | | | | | |
| Output Common Mode Voltage | | | 1.14 | | V |

| TIMING | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Aperture Delay | | 190 | | ps |
| RMS Aperture Jitter | | 100 | | fs |
| Synchronous Clock Divider Reset Recovery Time (DLL recovery time after Synchronous Reset) | | 250 | | µs |
| Latency (ADC Pipeline Delay) | | 10 | | cycles |
| Overvoltage Recovery | | 1 | | cycles |
| SERDES | | | | |
| PLL Lock Time | | 295 | | µs |
| PLL Bandwidth | | 2.2 | | MHz |
| Added Random Jitter | | 5 | | psRMS |
| Added Deterministic Jitter | | 7 | | ps P-P |
| Maximum Input Sample Clock Total Jitter to Maintain SERDES BER <1E-12 (1kHz - 10MHz carrier) | | 5 | | ps RMS |

| TIMING | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Clock Inputs | | | | |
| Inputs Common Mode Voltage | | 0.9 | | V |
| CLKP, CLKN Swing | | 1.8 | | V |
| LVDS Inputs | | | | |
| SYNCP, SYNCN Setup Time (with Respect to the Positive Edge of CLKP) | 400 | 75 | | ps |
| SYNCP, SYNCN Hold Time (with Respect to the Positive Edge of CLKP) | | 150 | 350 | ps |
| CML Outputs | | | | |
| Output Rise Time | | 165 | | ps |
| Output Fall Time | | 145 | | ps |
| Data Output Duty Cycle | | 50 | | % |
| Differential Output Resistance | | 100 | | Ω |
| Differential Output Voltage | | 760 | | mVP-P |
| SPI INTERFACE | | | | |
| SCLK Period Write operation | 7 | | | cycles |
| SCLK Period Read operation | 16 | | | cycles |
| CSB(Hi-Lo) to SCLK(Lo-Hi) Setup Time | 2 | | | cycles |
| CSB(Lo-Hi) after SCLK(Lo-Hi) Hold Time | 5 | | | cycles |
| Data Valid to SCLK(Lo-Hi) Setup Time | 6 | | | cycles |
| Data Valid after SCLK(Lo-Hi) Hold Time | 4 | | | cycles |
| Data Valid after SCLK(Hi-Lo) Time | | | 4 | cycles |

| POWER REQUIREMENTS | TEST CONDITION | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| 1.8V Analog Supply Voltage | | | 1.8 | | V |
| 1.8V Digital Supply Voltage | | | 1.8 | | V |
| 1.8V Analog Supply Current | | | 283 | 306 | mA |
| 1.8V Digital Supply Current | | | 109 | 122 | mA |
| Power Supply Rejection Ratio | 30MHz, 200mVP-P | | 38 | | dB |
| Normal Mode | | | 706 | 770 | mW |
| Nap Mode | | | 267 | 310 | mW |
| Sleep Mode | | | 6 | 14 | mW |
| Nap Mode Wakeup Time | | | 5 | | µs |
| Sleep Mode Wakeup Time | | | 1 | | ms |

## TECHNICAL NOTES

### Theory of Operation

The ADS-970 is based upon a 16-bit, 125MSPS ADC converter core that utilizes a pipelined successive approximation architecture. The input voltage is captured by a Sample-Hold Amplifier (S/H) and converted to a unit of charge. Proprietary charge-domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. Digital error correction is also applied.

### Power-On Calibration

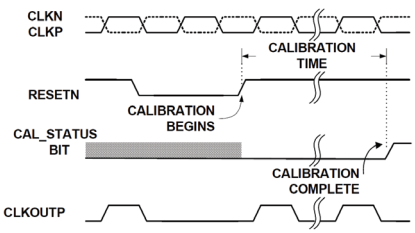
The ADC core(s) perform a self-calibration at start-up. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins must not be connected
- SDO has an internal pull-up and should not be driven externally
- RESETN is pulled low by the ADC internally during POR. External driving of RESETN is optional.
- SPI communications must not be attempted during calibration, with the only exception of performing read operations on the cal_done register at address 0xB6.

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

After the power supply has stabilized, the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. If a subsequent user-initiated reset is desired, the RESETN pin should be connected to an open-drain driver with an off-state/high impedance state leakage of less than 0.5mA to assure exit from the reset state so calibration can start.

The calibration sequence is initiated on the rising edge of RESETN, as shown in the figure below. Calibration status can be determined by reading the cal_ status bit (LSB) at 0xB6. This bit is '0' during calibration and goes to a logic '1' when calibration is complete. During calibration the JESD204 transmitter PLL is not locked to the ADC sample clock, so the CML outputs will toggle at an undetermined rate. Normal operation is resumed once calibration is complete.

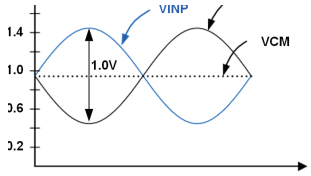



### User Initiated Reset

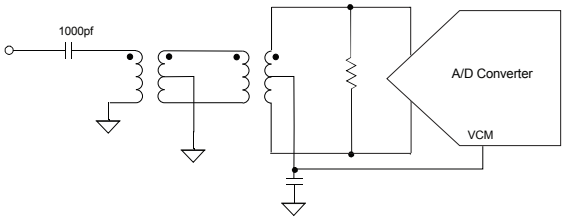
Recalibration of the ADC can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength in its high impedance state of less than 0.5mA is recommended, as RESETN has an internal high impedance pull-up to OVDD. As is the case during power-on reset, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

### Analog Input

A single fully differential input (VINP/VINN) connects to the sample and hold amplifier (SHA) of each unit ADC. The ideal full-scale input voltage is 2.0V, centered at the VCM voltage as shown in the figure below.




Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in the figure below.



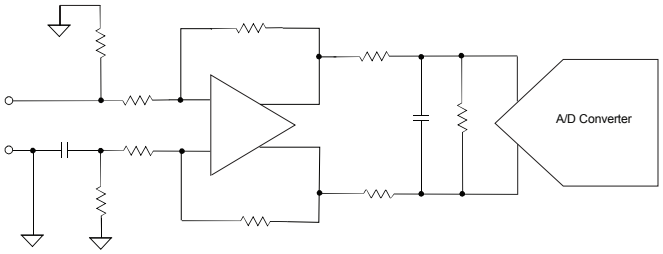

An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs.

The S/H amplifier design uses a switched capacitor input stage of the A/D, which creates current spikes when the sampling capacitance is reconnected to the input voltage. This causes a disturbance at the input, which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 2:1 or 1:1 transformer and low shunt resistance are recommended for optimal performance

When an over range occurs, the data sample output bits are held at full scale (all 0's or all 1's), thus allowing the detection of this condition in the receiver device.

## TECHNICAL NOTES

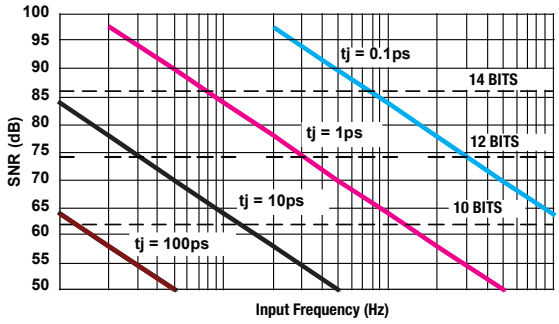
A differential amplifier, as shown in the simplified block diagram below, can be used in applications that require DC-coupling. In this configuration, the amplifier will typically dominate the achievable SNR and distortion performance.




### Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (tJ) and SNR is shown in Equation 1 and is illustrated in the figure below.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right)$$

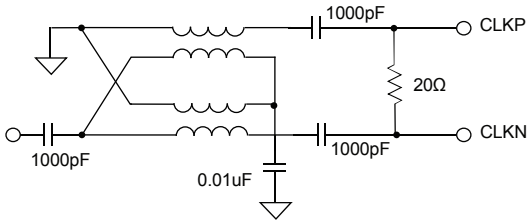



This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise as well. Internal aperture jitter is the uncertainty in the sampling instant. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

### Clock Input

The clock input circuit is a differential pair. Driving these inputs with a high level (up to 1.8VP-P on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels. The clock input is functional with AC-coupled LVDS, LVPECL, and CML drive levels. To maintain the lowest possible aperture jitter, it is recommended to have high slew rate at the zero crossing of the differential clock input signal.

The recommended drive circuit is shown in the figure below. A duty range of 40% to 60% is acceptable. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 through a Thevenin equivalent of 10kΩ to facilitate AC coupling.




A selectable 2x or 4x frequency divider is provided in series with the clock input. The divider can be used in the 2x mode with a sample clock equal to twice the desired sample rate or in 4x mode with a sample clock equal to four times the desired sample rate. Use of the 2x or 4x frequency divider enables the use of the Phase Slip feature, which enables the system to be able to select the phase of the divide by 2 or divide by 4 that causes the ADC to sample the analog input.

| CLKDIV PIN SETTINGS | |
|---|---|
| CLKDIV PIN | DIVIDE RATIO |
| Float | 1 |
| AVDD | 4 |
| Midscale | +2.500000 |
| –FS +1 LSB | -VREF + 1LSB |
| -FS | -VREF |

The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. If the frequency of the input clock changes, the DLL may take additioanl time regain lock. The lock time is inversely proportional to the sample rate.

The DLL has two ranges of operation, slow and fast. The slow range can be used for ADC core sample rates between 40MSPS and 100MSPS, while the default fast range can be used from 80MSPS to the maximum specified sample rate. The lane data rate is related to the ADC core sample rate by a relationship that is defined by the JESD204 transmitter configuration, and has additional frequency constraints.

## TECHNICAL NOTES

### Power Disipation

The power dissipated by the device is dependent on the ADC sample rate and the number of active lanes in the link. There is a fixed bias current drawn from the analog supply for the ADC, along with a fixed bias current drawn from the digital supply for each active lane. The remaining power dissipation is linearly related to the sample rate.

### Voltage Reference

A temperature compensated internal voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each ADC is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

### Digital Outputs

The digital outputs are in CML format, and feature analog and digital characteristics compliant with the JESD204 standard requirements

### Clock Divider Synchronous Reset

The function of clock divider synchronous reset is available as a SPI-programmable overloaded function on the SYNCP and SYNCN pins. Given that the clock divider reset and SYNC features have the same electrical and timing requirements, this overloading allows the system to generate only a single well timed signal with respect to the ADC sample clock and select the ADC's interpretation of the signal as a SPI-programmable option (see SPI register 0x77 description for more information). By default the SYNCP and SYNCN pins will function as the JESD204 SYNC~.

### JESD204 Transmitter

The conversion data is presented by a JESD204B-compliant SERDES interface. The SERDES lane data rate supports typical speeds up to 4.375Gbps, exceeding the 3.125Gbps maximum specified by the JESD204 rev A standard. A SYNC input is included, which is used for lane initialization as well as time alignment of multiple converter devices. AC coupling of the SERDES lane(s) on the board is required. For more information about the standardized characteristics and features of a JESD204 interface, please see JESD204 rev A and rev B standards.

### Soft Reset

Soft reset is a function intended to be used when the power on reset is to be re-run. An application may decide to issue a soft calibration command after significant temperature change or after a change in the sample rate frequency to optimize performance under the new condition.

Soft reset is issued by writing the Soft Reset bit at SPI address 0x00. Soft reset is a self-resetting bit in that will automatically return to 0 once the power on calibration has completed.

The power-down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. However, if the ADC is powered-on with the NAPSLP pin in either Nap or Sleep modes, the pin must be first set to Normal before the SPI port will be enabled. Therefore, before the SPI port can be used to override the NAPSLP pin setting, the ADC must have been put into Normal mode at least once using the NAPSLP pin. Further details on the SPI port are contained in "Serial Peripheral Interface".

### Data Format

Output data can be presented in three formats: two's complement (default), Gray code and offset binary. The data format can be controlled through the SPI port by writing to address 0x73. Details on this are contained in "Serial Peripheral Interface" on page 22.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.

| OUTPUT CODING | | | |
|---|---|---|---|
| INPUT VOLTAGE | OFFSET BINARY | TWO'S COMPLEMENT | GRAY CODE |
| –Full Scale | 00 0000 0000 0000 | 10 0000 0000 0000 | 00 0000 0000 0000 |
| –Full Scale +1LSB | 00 0000 0000 0001 | 10 0000 0000 0001 | 00 0000 0000 0001 |
| Mid–Scale | 10 0000 0000 0000 | 00 0000 0000 0000 | 11 0000 0000 0000 |
| +Full Scale – 1LSB | 11 1111 1111 1110 | 01 1111 1111 1110 | 10 0000 0000 0001 |
| +Full Scale | 11 1111 1111 1111 | 01 1111 1111 1111 | 10 0000 0000 0000 |

### Sleep / Nap Mode

Portions of the device may be shut down to save power during times when operation of the ADC is not required. Two power saving modes are available: Nap, and Sleep. Nap mode reduces power dissipation significantly while taking a very short time to return to functionality. Sleep mode reduces power consumption drastically while taking longer to return to functionality. In Nap mode the JESD204 lanes will continue to produce valid encoded data, allowing the link to remain active and thus return to a functional state quickly. The data transmitted over the lanes in nap mode is the last valid ADC sample, repeated until leaving nap mode. The 8b/10b encoder's running disparity will prevent the potentially long time repetition of this last valid sample from creating DC bias on the lane. In sleep mode the JESD204 lanes will be deactivated to conserve power. Thus, sometime after wake up code group alignment will be required to reestablish the link.

The input clock should remain running and at a fixed frequency during Nap or Sleep, and CSB should be high. The JESD204 link will only remain established during nap mode if the input clock continues to remain stable during the nap period.

By default after the device is powered on, the operational state is controlled by the NAPSLP pin as shown in the table on the following page. Please note that power on calibration occurs at power up time regardless of the state of the NAPSLP pin; immediately following this power on calibration routine the device will enter nap or sleep state if the NAPSLP pin voltage dictates it is to do so.

## TECHNICAL NOTES

| NAPSLP PIN SETTING TABLE | |
|---|---|
| NAPSLP Pin | Mode |
| AVSS | Normal |
| Float | Nap |
| AVDD | Sleep |

### Initial Lane Alignment

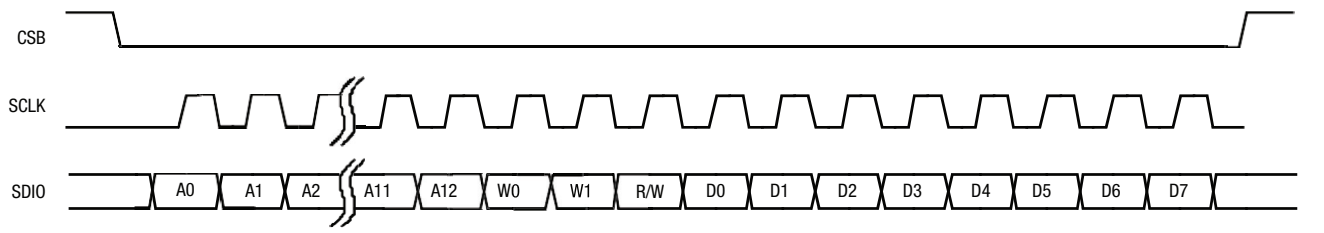
The link initialization process is started by asserting the SYNC~ signal to the ADC device. This assertion causes the JESD204 transmitter to generate comma characters, which are used by the receiver to accomplish code group synchronization (bit and octet alignment, respectively). Once code group synchronization is detected in the receiver, it de-asserts the SYNC~ signal, causing the JESD204 transmitter to generate the initial lane alignment sequence (ILA). The ILA is comprised of 4 multi-frames of data in a standard format, with the length of each multi-frame determined by the K parameter as programmed into the SPI JESD204 parameter table. The ILA includes standard control character markers that can be used to perform channel bonding in the receiving device if desired. The 2nd multi-frame includes the full JESD204 parameter data, allowing the receiver to auto-detect the lane configuration if desired.

After completion of the ILA the JESD204 transmitter begins transmitting ADC sample data. Continuous link and lane alignment monitoring is accomplished via an octet substitution scheme. The last octet in each frame, if identical to the last octet in the previous frame, is replaced with a specific control character. If both sides of the link support lane synchronization, the last octet in each multi-frame, if identical to the last octet in the previous frame, is replaced with a different specific control character. A more complete description of the link initialization sequence, including finite state machine implementation, can be found in the JESD204 rev A standard.

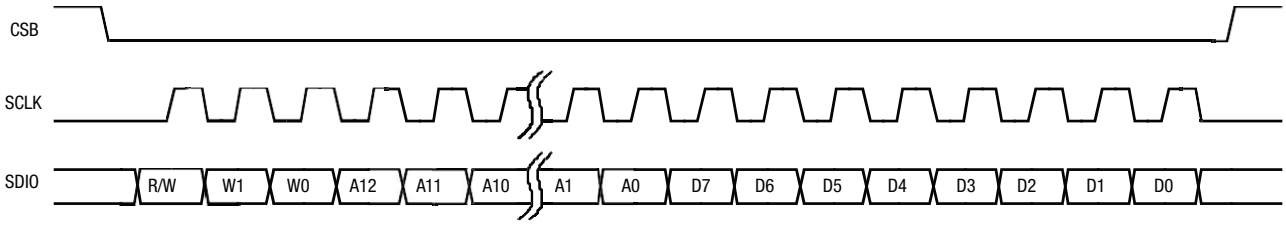
### Lane Data Rate

The lane data rate for this product family is constrained to be greater than or equal to 1Gbps and less than or equal to 3.125Gbps for guaranteed operation, so as to be consistent with the lane data rate limit of 3.125Gbps set by the JESD204 rev A standard. The lane data rate can typically exceed 4.2Gbps for this product family.

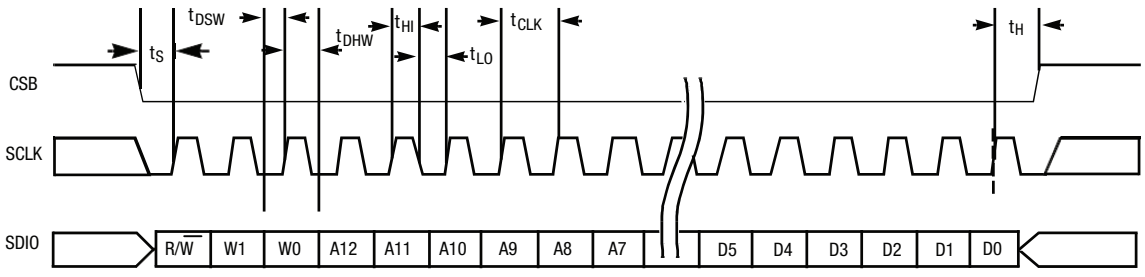
## TIMING




LSB FIRST ADDRESSING

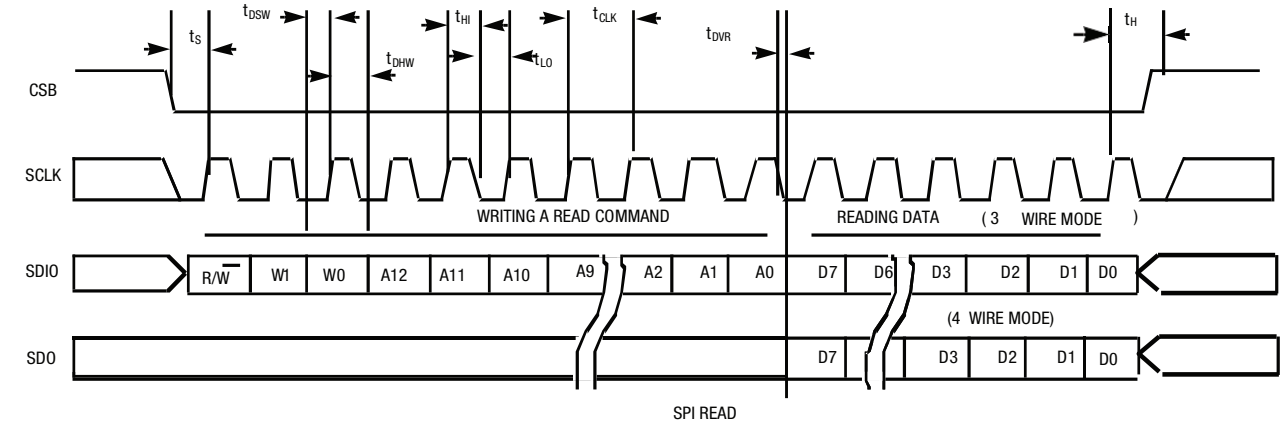


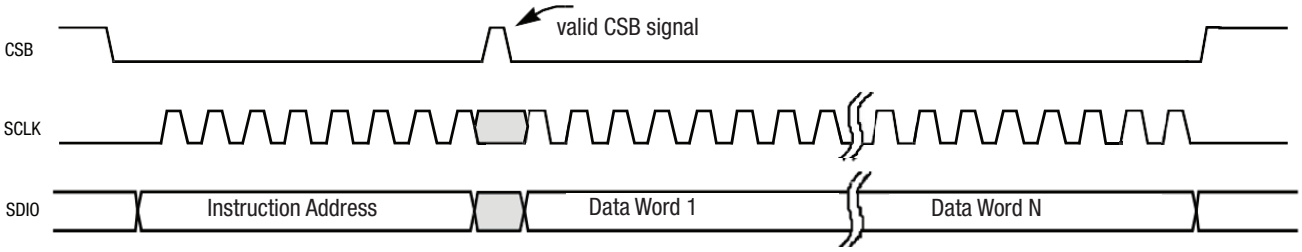

MSB FIRST ADDRESSING



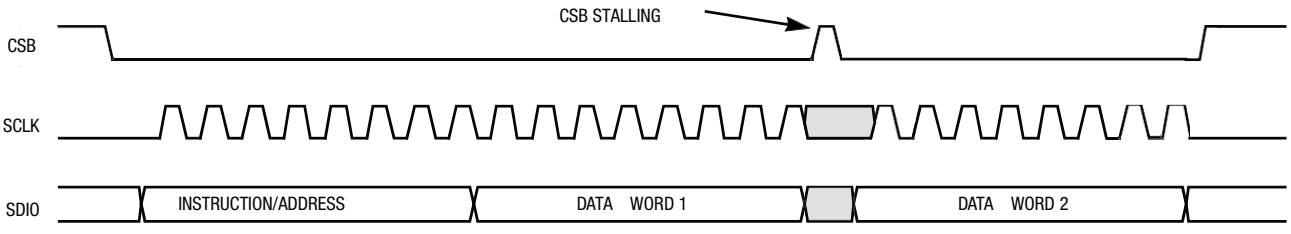

SPI WRITE

## TIMING




**N-BYTE TRANSFER**




**2-BYTE TRANSFER**

## TECHNICAL NOTES

### Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) serial data output (SDO), and serial data input/output (SDIO). The maximum SCLK rate is equal to the ADC sample rate (fSAMPLE) divided by 7 for write operations and fSAMPLE divided by 16 for reads. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

### SPI Physical Iterface

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin in three-wire mode. The state of the SDIO pin is set automatically in the communication protocol (described in the following). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in four-wire mode. The SPI port operates in a half duplex master/slave configuration, with the ADC functioning as a slave. Multiple slave devices can interface to a single master in three-wire mode only, since the SDO output of an unaddressed device is asserted in four wire mode.

The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time (again, only in three-wire mode). If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high-to-low transition on CSB determines the beginning of the two-byte instruction/address command; SCLK must be static low before the CSB transition. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. The Timing Waveforms show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode, the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented. In the default mode, the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table below). The lower 13 bits contain the first address for the data transfer.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the ADC (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed to stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

| BYTE TRANSFER SELECTION | |
|---|---|
| [W1:W0] | BYTES TRANS-FERRED |
| 00 | 1 |
| 01 | 2 |
| 10 | 3 |
| 11 | 4 or more |

### Address 0x00:Chip_Port_Config

Portions of the device may be shut down to save power during times when Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various micro controllers.

Bit 7 SDO Active Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values. Bit 4 Reserved This bit should always be set high.

Bits 3:0 These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

### Address 0x02:Burst_End

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. The burst is ended by pulling the CSB pin high. Setting the burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.

### Address 0x08:Chip_ID
### Address 0x09:Chip_Version
### Address 0x20:Offset_Coarse_ADC0
### Address 0x21:Offset_Fine_ADC0

The input offset of the ADC core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in the table below. The data format is twos complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the

register value then write the incremented or decremented value back to the same register.

| OFFSET ADJUSTMENT TABLE | | |
|---|---|---|
| PARAMETER | 0x20[7:0] COARSE OFFSET | 0x21[7:0] FINE OFFSET |
| Steps | 255 | 255 |
| –Full Scale (0x00) | -133LSB (-47mV) | -5LSB (-1.75mV) |
| Mid–Scale (0x80) | 0.0LSB (0.0mV) | 0.0LSB |
| +Full Scale (0xFF) | +133LSB (+47mV) | +5LSB (+1.75mV) |
| Nominal Step Size | 1.04LSB (0.37mV) | 0.04LSB (0.014mV) |

## TECHNICAL NOTES

### Address 0x22:Gain_Coarse_ADC0
### Address 0x23:Gain_Medium_ADC0
### Address 0x24:Gain_Fine_ADC0

Gain of the ADC core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2%. ('0011' ≈ -4.2% and '1100' ≈ +4.2%) It is recommended to use one of the coarse gain settings (-4.2%,-2.8%, -1.4%, 0, 1.4%, 2.8%, 4.2%) and fine-tune the gain using the registers at 0x0023 and 0x24.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

| COARSE GAIN ADJUST TABLE | |
|---|---|
| 0x22[3:0] core 0<br>0x26[3:0] core 1 | NOMINAL COARSE GAIN ADJUST (%) |
| Bit 3 | +2.8 |
| Bit 2 | +1.4 |
| Bit 1 | -2.8 |
| Bit 0 | -1.4 |

| MEDIUM AND FINE GAIN ADJUST TABLE | | |
|---|---|---|
| PARAMETER | 0x20[7:0] COARSE OFFSET<br>0x23[7:0] MEDIUM GAIN | 0x21[7:0] FINE OFFSET<br>0x24[7:0] FINE GAIN |
| Steps | 256 | 256 |
| –Full Scale (0x00) | -2% | -0.20% |
| Mid–Scale (0x80) | 0.00% | 0.00% |
| +Full Scale (0xFF) | +2% | +0.2% |
| Nominal Step Size | 0.016% | 0.0016% |

### Address 0x25:Modes

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes. This functionality can be overridden and controlled through the SPI. However, if the ADC is powered-on with the NAPSLP pin in either Nap or Sleep modes, the pin must first be set to Normal before the SPI port will be enabled. Therefore, before the SPI port can be used to override the NAPSLP pin setting, the ADC must have been put into Normal mode at least once using the NAPSLP pin. This register is not changed by a Soft Reset.

### Address 0x26:Offset_Coarse_ADC1
### Address 0x27:Offset_Fine_ADC1

The input offset of ADC core#1 can be adjusted in fine and coarse steps in the same way that offset for core#0 can be adjusted. Both adjustments are made via an 8-bit word as detailed in the table below. The data format is two's complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

### Address 0x28:Gain_Coarse_ADC1
### Address 0x29:Gain_Medium_ADC1
### Address 0x2A:Gain_Fine_ADC1

Gain of ADC core #1 can be adjusted in coarse, medium and fine steps in the same way that core #0 can be adjusted. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. Multiple Coarse Gain Bits can be set for a total adjustment range of ±4.2.

### Global Device Configuration/Control

### Address 0x71:Phase_Slip

When using the clock_divide feature, the sample clock edge that the ADC uses to sample the analog input signal can be one of several different edges on the incoming higher frequency sample clock. For example, in clock_divide = 2 mode, every other incoming sample clock edge gets used by the ADC to sample the analog input. The phase_slip feature allows the system to control which edge of the incoming sample clock signals gets used to cause the sampling event, by "slipping" the sampling event by one input clock period each time phase_slip is asserted.

The clkdivrst feature can work in conjunction with phase_slip. After well-timed assertion of the clkdivrst signal (via overloading on the SYNC inputs), the sampling edge position with respect to the incoming clock rate will have been reset, allowing the system to "slip" whatever desired number of incoming clock periods from a known state.

### Address 0x72:Clock_Divide

The ADC has a selectable clock divider that can be set to divide by two or one (no division). By default, the tri-level CLKDIV pin selects the divisor This functionality can be overridden and controlled through the SPI, as shown in the table below. This register is not changed by a Soft Reset.

| CLOCK DIVIDER SELECTION TABLE | |
|---|---|
| VALUE | 0x72[2:0] CLOCK DIVIDER |
| ¬¬000 | Pin Control |
| 001 | Divide by 1 |
| 010 | Divide by 2 |
| other | Not Allowed |

### Address 0x73:Output_Mode_B

Bit 6 DLL Range

This bit sets the DLL operating range to fast (default) or slow.

Internal clock signals are generated by a delay-locked loop (DLL), which has a finite operating range. The table below shows the allowable sample rate ranges for the slow and fast settings.

| DLL RANGE SELECTION TABLE | | | |
|---|---|---|---|
| DLL RANGE | MIN | MAX | UNIT |
| Slow | 40 | 100 | MSPS |
| Fast | 80 | 125 | MSPS |

## GLOSSARY OF SPECIFICATIONS

**DIFFERENTIAL LINEARITY ERROR**: The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of FSR/2n.

**DIFFERENTIAL LINEARITY TEMPCO:** The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

**GAIN ERROR:** The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.
For +FS, This is the deviation of the last code transition (011...110 to 011...111) from the ideal (+INPUT) - (-INPUT) (i.e., +REF – 1 LSB), after the zero code error has been adjusted out.
For -FS, this is the deviation of the first code transition (100...000 to 100...001) from the ideal (+INPUT) - (-INPUT) (i.e., – REF + 1 LSB), after the zero code error has been adjusted out.

**GAIN TEMPCO:** The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

**INTEGRAL LINEARITY ERROR:** The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

**INTERNAL REFERENCE VOLTAGE DRIFT:** The maximum deviation from the measured value at room temperature as compared with the value measured at either Tmin or Tmax.

**OFFSET ERROR:** The deviation from the ideal at analog zero output. This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal (+INPUT) - (-INPUT) (i.e., 0 LSB).

**OFFSET DRIFT:** The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

**POWER SUPPLY REJECTION RATIO (PSRR):** The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

**SETTLING TIME:** The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and Sample-Holds and D/A converters.

**SPURIOUS FREE DYNAMIC RANGE (SFDR):** The largest harmonic, spurious frequency or noise component in a signal FFT. It is expressed in db with respect to the fundamental frequency.

**SIGNAL TO NOISE RATIO AND DISTORTION (SINAD):** Usually expressed in dB. It is the ratio of the rms of the fundamental signal amplitude taking at -0.5 dB below full scale to the rms of all the noise spectral components generated by an A/D including all the Harmonics.

**SIGNAL TO NOISE RATIO (SNR):** Usually expressed in dB. It is the ratio of the rms of the fundamental signal amplitude taking at -0.5 dB below full scale to the rms of all the noise spectral components generated by an A/D excluding the first five Harmonics.

**TOTAL HARMONIC DISTORTION:** The ratio of the rms sum of the Harmonics to the rms of the fundamental signal. It is usually expressed in dB.

**TWO TONE INTERMODULATION DISTORTION:** The change in a sinusoidal waveform that is caused by the presence of a second sinusoidal input of a different frequency. Typically specified in dB.

**ACQUISITION TIME:** For a sample-hold, the time required, after the sample command is given, for the hold capacitor to charge to a full scale voltage change and then remain within the specified error band of ±1/2 LSB.

**APERTURE DELAY TIME:** In a sample-hold, the time elapsed from the hold command to the actual opening of the sampling switch.

**APERTURE JITTER:** See Aperture uncertainty time

**APERTURE TIME:** The time window, or time uncertainty, in making a measurement. For an A/D converter the conversion time; for a sample- hold it is the signal averaging time during the sample to hold transition.

**APERTURE UNCERTAINTY TIME:** In a sample-hold, the time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample

**COMMON MODE REJECTION RATIO:** is defined as the ratio of power of the A/D at FS max to the power of a 250mVpp sine wave applied to +INPUT and -INPUT, generally expressed in dB.

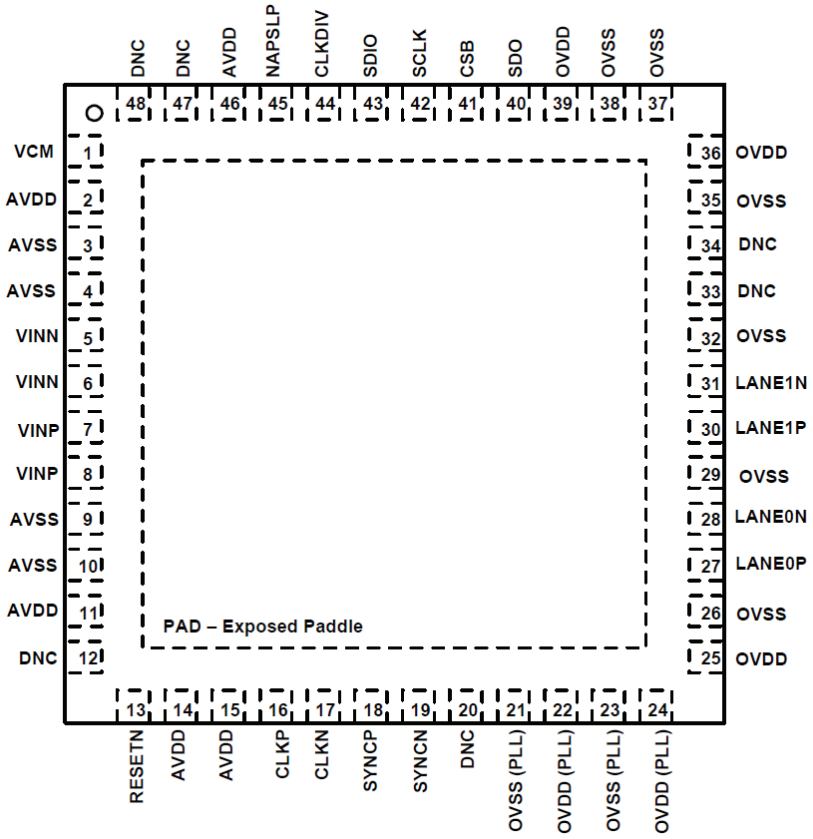
$$CMRR = 20 \log 10\ AD\ /ACM$$

where AD is the power of the A/D at FS and ACM is the power of the 250mVpp sine wave applied to +INPUT and -INPUT.

## ORDERING INFORMATION

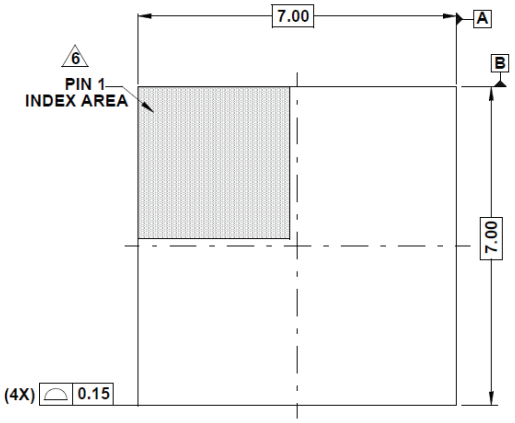
| ORDERING INFORMATION | | | |
|---|---|---|---|
| MODEL NUMBER | OPERATING TEMP. RANGE (°C) | PACKAGE | SHIPPING |
| ADS-970SE | -40 to +105 | 48 Pin Leadless Plastic Quad Flat Package | Tube |
| ADS-970SM | -55 to +125 | 48 Pin Leadless Plastic Quad Flat Package | Tube |

| PIN DESCRIPTIONS | | |
|---|---|---|
| PIN | PIN NAME | DESCRIPTION |
| PIN NUMBER | NAME | FUNCTION |
| 2, 11, 14, 15, 46 | AVDD | 1.8V Analog Supply |
| 12, 20, 33, 34, 47, 48 | DNC | Do Not Connect |
| 3, 4, 9, 10 | AVSS | Analog Ground |
| 7, 8 | VINP | Analog Input, Positive |
| 5, 6 | VINN | Analog Input, Negative |
| 1 | VCM | Common Mode Output |
| 44 | CLKDIV | Clock Divider Control |
| 16, 17 | CLKP, CLKN | Clock Input True, Complement |
| 45 | NAPSLP | Power Control (Nap, Sleep modes) |
| 13 | RESETN | Power On Reset (Active Low) |
| 26, 29, 32, 35, 37, 38 | OVSS | Output Ground |
| 25, 36, 39 | OVDD | 1.8V Digital Supply |
| 22, 24 | OVDD (PLL) | 1.8V Analog Supply for SERDES PLL |
| 21, 23 | OVSS (PLL) | Analog Ground Supply for SERDES PLL |
| 18, 19 | SYNCP, SYNCN | JESD204 SYNC Input |
| 27, 28 | LANE0P, LANE0N | SERDES Lane 0 |
| 30, 31 | LANE1P, LANE1N | SERDES Lane 1 |
| 40 | SDO | SPI Serial Data Output |
| 41 | CSB | SPI Chip Select (active low) |
| 42 | SCLK | SPI Clock |
| 43 | SDIO | SPI Serial Data Input/Output |
| PAD | AVSS | Exposed Paddle. Analog Ground (connect to AVSS) |

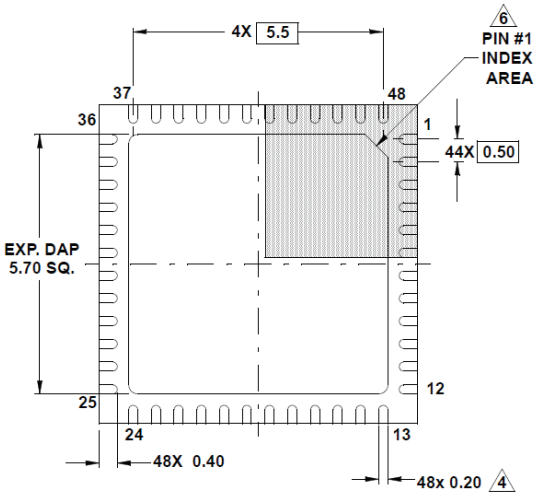


## MECHANICAL DIMENSIONS

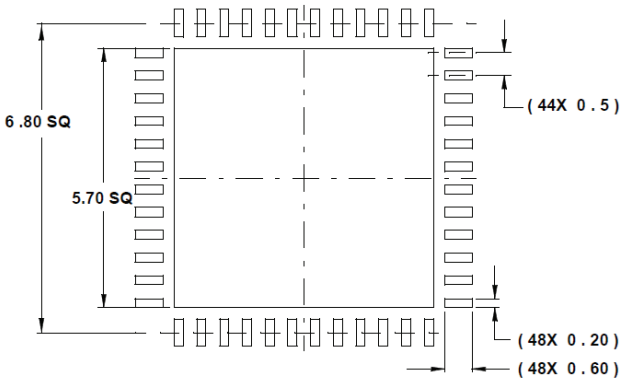
**48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 0, 1/10**



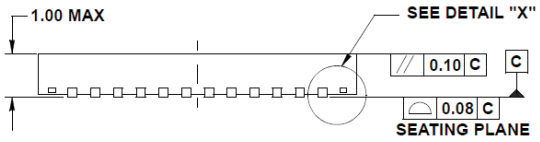

TOP VIEW



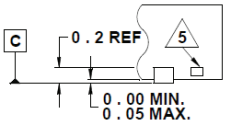

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.