

APPLICATION INFORMATION

The SPPL12420RH is a monolithic synchronous buck regulator featuring integrated 110 mΩ Power MOSFETs that can provide up to 2 A of load current. It regulates input voltages from 4.5 V to 24 V down to an output voltage as low as 0.923 V while providing soft-start, cycle-by-cycle over-current, under-voltage lockout and over-temperature protection.

This section of the datasheet describes typical application circuits, provides recommendations on component selection, and discusses thermal and layout design considerations.

TYPICAL APPLICATIONS

The SPPL12420RH uses a fixed frequency, current-mode step-down regulator architecture to deliver constant voltage to the load. Figure 9 shows a typical application circuit.

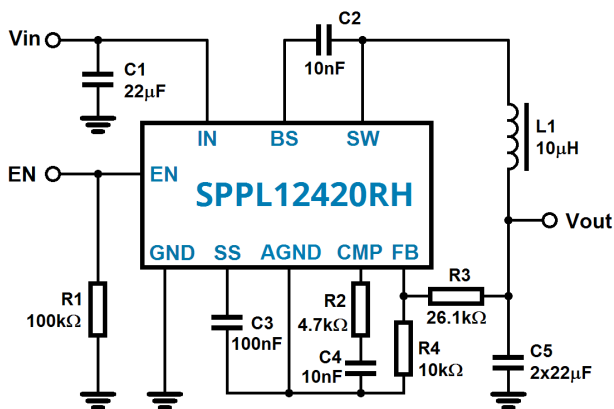


Figure 9. Typical Application Circuit

The circuit of Figure 9 takes an input voltage between 4.5 V and 24 V and regulates it down to 3.3 V while delivering 2 A of load current.

SETTING THE OUTPUT VOLTAGE

Based on the circuit of Figure 9, the output voltage depends on the feedback voltage V_{FB} and the resistor divider network consisting of R_3 and R_4 , as expressed with the following equation:

$$V_{OUT} = V_{FB} \cdot \frac{R_3 + R_4}{R_4}$$

The R_4 resistor value may be as high as 100 kΩ, however 10 kΩ resistor value is typically recommended. Given this and the typical V_{FB} of 0.923 V, the R_3 resistor may easily be calculated for a desired output voltage. Table 1 exemplifies several standard resistor values needed to achieve desired output voltage. If standard resistor values are not available a parallel combination of two standard resistors may also be used.

V_{OUT} [V]	R_3 [kΩ]	R_4 [kΩ]
1.0	0.825	10
1.2	3.01	10
1.8	9.53	10
2.5	16.9	10
3.3	26.1	10
5	44.2	10

Table 1. Examples of R3/R4 for Typical Output Voltages

COMPONENT SELECTION

Inductor: The operation frequency of the SPPL12420RH allows the use of small surface mount inductors. The minimum inductance value is inversely proportional to the operating frequency and is bounded by the following limits:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{f_S \cdot I_{L(MAX)ripple} \cdot V_{IN}} [H]$$

where

- f_S = Operating frequency [Hz]
- $I_{L(MAX)ripple}$ = Allowable max inductor current ripple [A]
- V_{IN} = Input voltage [V]
- V_{OUT} = Output voltage [V]

The inductor current ripple is typically set to 20% to 40% of the maximum load current. Given this, the operating frequency and the input and output voltages for the SPPL12420RH regulator circuit, it is easy to calculate the optimal inductor value which typically ranges between 10 and 47 μ H. Note that a larger value inductor will result in less ripple current and ultimately in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current is given in the following equation:

$$I_{L(peak)} = I_{LOAD} + \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{2 \cdot f_S \cdot L \cdot V_{IN}} [A]$$

For high efficiency, it is recommended to select an inductor with a high frequency core material (e.g. ferrite) to minimize core losses. Low ESR (equivalent series resistance) is another preferred inductor characteristic when designing for low losses. The inductor must handle the peak inductor current at full load without saturating. Note that the peak inductor current must be below the maximum switch current limit. Chip inductors typically do not have enough core to support the peak inductor currents above 1 A and are not suitable for the SPPL12420RH applications.

Lastly, select a toroid, pot core or shielded bobbin inductor for low radiated noise.

Optional Schottky Diode: During the transition between the high-side switch and the low side switch, the body diode of the low-side switch (N-channel power MOSFET) conducts the inductor current. The forward voltage of this body diode is relatively high. Therefore, an optional Schottky diode may be paralleled between SW and GND pins. The Schottky diode which features low forward voltage and fast recovery time will result in improved peak efficiency of the buck regulator circuits. The connection of the optional Schottky diode (D1) is shown in Figure 10.

Input Capacitor: The input current to the buck regulator is discontinuous, therefore, a capacitor is required to supply AC current to the regulator while maintaining the DC input voltage.

The input capacitor of Figure 9 (C1) absorbs the input switching current, therefore, it requires adequate ripple current rating. The RMS current in the input capacitor can be estimated using the following equation:

$$I_{CI} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case condition occurs when V_{IN} is twice the value of V_{OUT} . In this case, the I_{CI} is equal to the half of the load current. As a rule of thumb, select the input capacitor with the RMS current rating greater than the half of the maximum load current.

The input capacitor reduces peak currents drawn from the input source and reduces input switching noise. The input voltage ripple caused by the input capacitor can be estimated using the following equation:

$$dV_{IN} = \frac{I_{LOAD}}{C_1 \cdot f_S} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The input capacitor values in the range between 10 and 47 μ F are sufficient in most cases. Low ESR capacitors are recommended for a low loss operation. Ceramic capacitors with X5R or X7R dielectrics are preferred, however, tantalum and electrolytic capacitors are acceptable as well. When using electrolytic or tantalum capacitors, a small (e.g. 0.1 μ F), ceramic capacitors should also be used and placed as close to the IN pin as possible.

Output Capacitor: The value of the output capacitor of Figure 9 (C5) has an effect on the output voltage ripple as expressed in the following equation:

$$dV_{OUT} = \frac{V_{OUT}}{f_S \cdot L_1} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(ESR_{C5} + \frac{1}{8 \cdot f_S \cdot C_5}\right)$$

where

- f_S = Operating frequency [Hz]
- ESR_{C5} = Equivalent series resistance of C5
- V_{IN} = Input voltage [V]
- V_{OUT} = Output voltage [V]

The output capacitor C5 can be ceramic, tantalum or electrolytic type. When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, therefore, the above equation may be simplified as the following:

$$dV_{OUT} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \frac{V_{OUT}}{8 \cdot f_S^2 \cdot C_5 \cdot L_1}$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency, therefore, the original output voltage ripple equation can be re-written as the following expression:

$$dV_{OUT} = \frac{V_{OUT}}{f_S \cdot L_1} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot ESR_{C5}$$

To provide low output voltage ripple a minimum output capacitor value of 40 μ F is recommended.

Compensation Components: The SPPL12420RH employs current mode control for easy compensation and fast transient response. System stability and transient response are controlled via CMP pin. CMP pin is the output of the internal transconductance error amplifier. A series RC network (C4 and R2 of Figure 9) sets a pole-zero combination and controls the characteristics of the control system. The DC gain of the voltage feedback loop is given by the following equation:

$$A_{VDC} = R_{LOAD} \cdot G_{CS} \cdot A_{EA} \cdot \frac{V_{FB}}{V_{OUT}}$$

where

- G_{CS} = Current sense transconductance
- A_{EA} = Error amplifier voltage gain

The system has two poles of importance. One is due to the compensation capacitor (C4 of Figure 9) and the output resistor of the error amplifier. The other one is due to output capacitor (C5 of Figure 9) and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \cdot C_4 \cdot A_{EA}}$$

$$f_{P2} = \frac{1}{2\pi \cdot C_5 \cdot R_{LOAD}}$$

where

- G_{EA} = Error amplifier transconductance

The system has one zero of importance, due to the compensation capacitor (C4) and the compensation resistor (R2). The zero is located at:

$$f_{Z1} = \frac{1}{2\pi \cdot C_4 \cdot R_2}$$

The system may also have another zero of importance due to high output capacitance and ESR of C5 (output capacitor of Figure 9). The zero is located at:

$$f_{Z2} = \frac{1}{2\pi \cdot C_5 \cdot ESR_{C5}}$$

The C6 may be added to compensate for the ESR of C5. The C6 together with R2 creates another pole which is located at:

$$f_{p3} = \frac{1}{2\pi \cdot C_6 \cdot R_2}$$

The aim of the compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system to be unstable. As a rule of thumb, the crossover frequency (f_c) below one tenth of the switching frequency is recommended. This is expressed by the following inequality:

$$f_c < \frac{f_s}{10}$$

The following steps may be used for optimizing the compensation components:

1. Select the compensation resistor, R2 to set the desired crossover frequency. The R2 resistor value can be determined using the following equation:

$$R_2 = \frac{2\pi \cdot C_5 \cdot f_c \cdot V_{OUT}}{G_{EA} \cdot G_{CS} \cdot V_{FB}}$$

2. Select the compensation capacitor C4 to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{z1} , below one quarter of the crossover frequency provides sufficient phase margin. The C4 capacitor value can be determined using the following inequality:

$$C_4 > \frac{4}{2\pi \cdot R_2 \cdot f_c}$$

3. Determine if the second compensation capacitor, C6, is needed. It is needed if the ESR zero (f_{z2}) of the output capacitor (C5) is located at less than half of the switching frequency as expressed in the following inequality:

$$\frac{f_s}{2} > \frac{1}{2\pi \cdot C_5 \cdot ESR_{C5}}$$

If the above inequality is valid, add the second compensation capacitor, C6, to set the third pole, f_{p3} , at the location of the ESR zero, f_{z2} . The C6 capacitor value can be determined using the following equation:

$$C_6 = \frac{C_5 \cdot ESR_{C5}}{R_2}$$

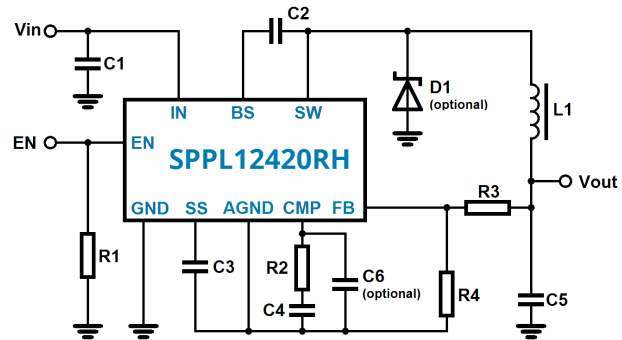
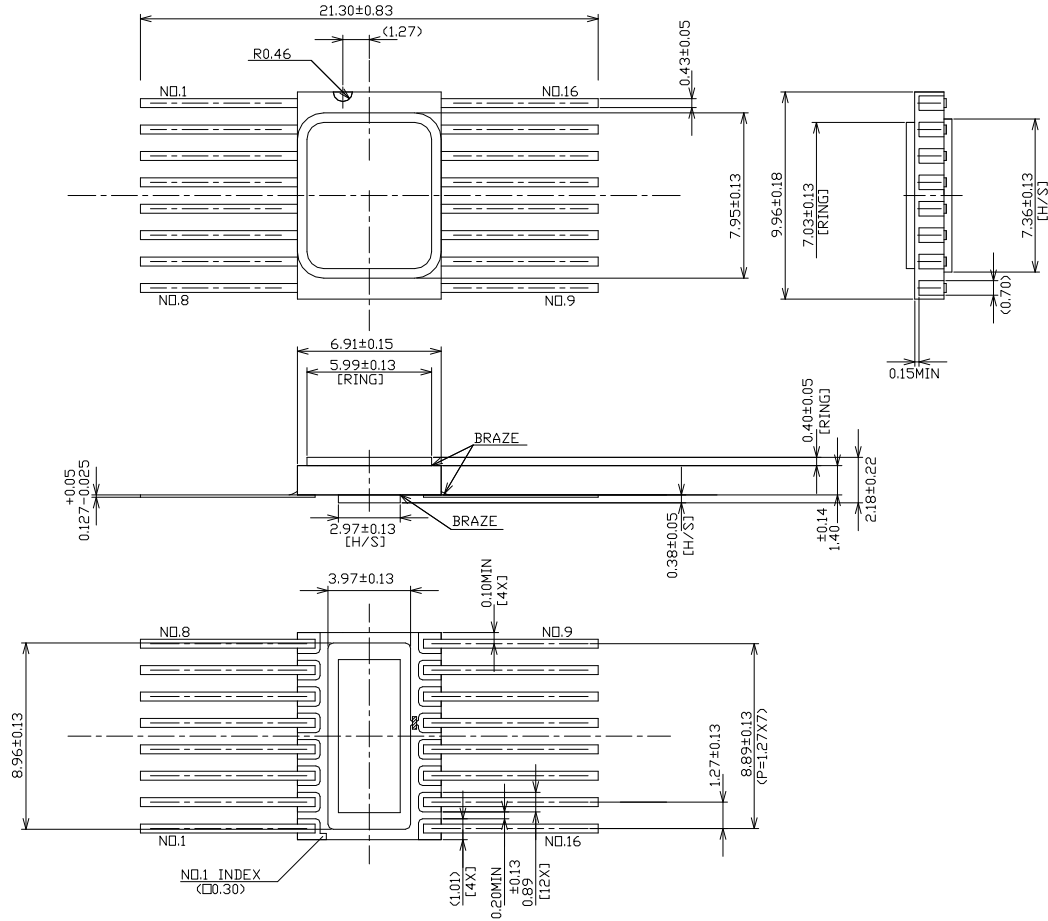


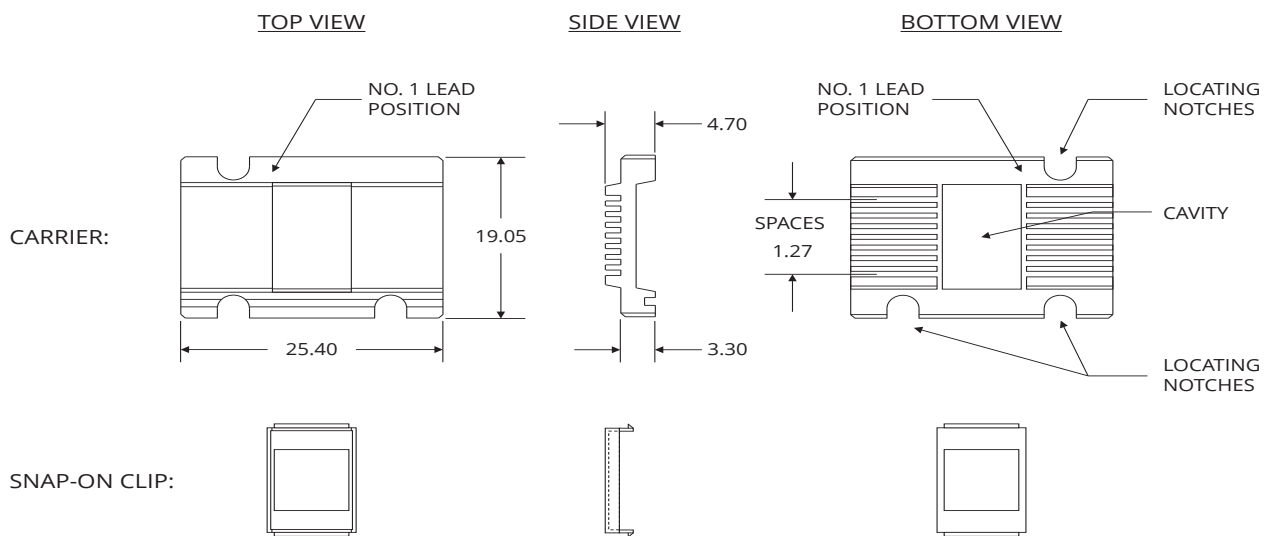
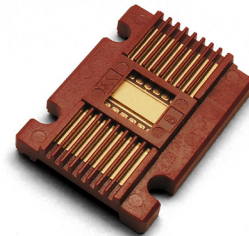
Figure 10. Application Circuit with Optional C6 and Optional D1 Schottky Diode

PACKAGE DIMENSION (16-LEAD FLATPACK)



PROTECTIVE CARRIER

The SPPL12420RH is delivered in a plastic carrier for mechanical protection.



IMPORTANT NOTICE

The information contained in this document is believed to be accurate at the time of printing. SPACE IC reserves the right to make changes to its products or specifications without notice, however, and assumes no responsibility or liability for the use of its products; nor does the purchase, lease, or use of a product or service from SPACE IC convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual rights of SPACE IC or of third parties. Please visit our website for the most recent revision of this datasheet or contact info@space-ic.com. Customers are responsible for their products and applications using SPACE IC products.

Resale of SPACE IC products or services with statements different from or beyond the parameters stated by SPACE IC for that product or service voids all express and any implied warranties for the associated SPACE IC product or service. SPACE IC is not responsible or liable for any such statements.

© 2021 SPACE IC GmbH. All rights reserved. Information and data in this document are owned by SPACE IC and may not be edited, reproduced or redistributed in any way without written consent from SPACE IC.